Amorphous silicon detector and thin film transistor technology for large-area imaging of X-rays

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Abstract

This paper reviews amorphous silicon imaging technology in terms of the detector operating principles, electrical and optoelectronic characteristics, and stability. Also, issues pertinent to thin film transistor stability are presented along with optimization of materials and processing conditions for reduced \( V_T \)-shift and leakage current. Selected results are shown for X-ray and optical detectors, thin film transistors, and integrated X-ray pixel structures. Extension of the current fabrication processes to low (\( \leq 120^\circ \text{C} \)) temperature, enabling fabrication of thin film electronics on flexible (polymer) substrates, are also discussed along with preliminary results. © 2000 Elsevier Science Ltd. All rights reserved.

Keywords: Amorphous silicon technology; Thin film transistors; Imaging arrays

1. Introduction

Current interests in hydrogenated amorphous silicon (a-Si:H) technology extend well beyond active matrix liquid crystal displays and solar cells, and they stem from the variety of desired material and technological attributes [1,2]. The high optical absorption, low temperature deposition (<300°C), high uniformity over large area, few constraints on substrate size, material, or topology, standard integrated circuit (IC) lithography processes, and low capital equipment cost, associated with the a-Si:H material, offer a viable technological alternative for improved imaging of optical signals and high energy radiation. Notable application areas include: contact imaging for document scanning, digital copiers, and fax machines; color sensors/imaging; position/motion detection; radiation detection/imaging of high energy X-rays in biomedical applications, gamma-ray space telescopes, airport security systems, and non-destructive testing of mechanical integrity of materials or structures.

For large-area imaging of X-rays, different detection schemes can be employed. One configuration employs a phosphor layer which converts X-rays into visible photons; the latter being detected by a-Si:H photosensors [2]. This arrangement had shown good success at high X-ray energies. An alternative arrangement uses a photoconductor such as bulk amorphous selenium (a-Se) for photoelectric conversion [3]. Here, detection requires high electric fields (\( \sim \text{kV} \) operation) where there is efficient electron–hole separation and collection. More recently, we presented a low voltage direct detection scheme using Mo/a-Si:H Schottky diodes [4] (see Fig. 1). Here, interaction of X-ray photons with Mo leads to ejection of high energy electrons, by virtue of the photoelectric effect, into a reverse-biased a-Si:H depletion layer, where electron (avalanche) multiplication yields a gain. The pixel fabrication process is fully compatible with the a-Si:H thin film transistor (TFT) [5,6] intended to serve as a switching element for charge readout.

2. Heavy metal/a-Si:H Schottky diodes for direct detection of X-rays

The fabrication process of the Schottky diode is described in Fig. 2. First, a thin (100 nm) chromium (Cr) layer is sputter deposited on a glass wafer and patterned with mask 1, followed by plasma enhanced chemical vapor deposition (PECVD) of highly doped amorphous silicon (n⁺ a-Si:H) and intrinsic amorphous silicon (i-a-Si:H) layers in one pump-down to preserve the interface quality. The thicknesses of n⁺ a-Si:H and i-a-Si:H are 100 nm and 1 μm, respectively. The n⁺ a-Si:H layer is deposited to
provide an ohmic contact with the bottom electrode metal. Then, a heavy metal (in this case, Mo) is deposited to form the Schottky barrier interface and patterned with mask 2. Mask 3 patterns the top amorphous silicon nitride (a-SiNₓ) layer which is used as the etch stop against KOH solution which etches the amorphous silicon layers. Finally, mask 4 is used to open the contact windows on the top nitride layer where needed. The deposition parameters of the various thin films are listed in Table 1.

The choice of the top electrode material needs to take into consideration X-ray absorption, electron ejection, and the intrinsic mechanical stress. The stress in thin films will be discussed in more detail later in association with pixel configurations. The work function of the heavy metal determines the Schottky barrier height, which is crucial in that it determines the detector leakage. The leakage current of Mo/a-Si:H Schottky diode is shown in Fig. 3.

The thickness of the (top electrode) heavy metal is based on a compromise between the absorption of X-rays and the ejection of the energetic electrons from the metal into the depletion layer. Shown in Fig. 4 is the number of measured electrons over the X-ray source voltage of 40–100 kVp.

3. ITO/a-Si:H Schottky diodes for detection of optical signals

Another method of imaging X-rays is to convert the X-ray photons into visible light with a scintillating (phosphor) layer, followed by detection of the visible light with amorphous silicon photosensors. Here, we developed a room temperature indium tin oxide (ITO) process [7] for realization of a Schottky photodiode [8]. The device schematic and operating principle are illustrated in Fig. 5.

The fabrication of the ITO/a-Si:H Schottky photodiode is based on deposition of polycrystalline indium tin oxide at room temperature. Here, the ITO resistivity is below 6 x 10⁻⁴ Ω cm and optical transmittance of the film, within the range of visible wavelengths, is in excess of 80% [7]. We start with a 120-nm Cr layer which acts as the bottom electrode, followed by deposition of a highly doped n⁺ a-Si:H layer (thickness 50 nm) for ohmic contact. Thick (1 μm) intrinsic a-Si:H is then deposited to serve as the active layer. For all devices, the a-Si:H is etched in buffered HF to remove any surface oxide before the samples are loaded into the sputtering system. Polycrystalline ITO (thickness 80 nm) is then deposited in pure argon at room temperature for the Schottky contact and light window.

Fig. 6 shows the I–V characteristics of the ITO/a-Si:H Schottky photodiode. We observe that the dark current at a reverse bias of −2 V is low (≈7 x 10⁻¹⁰ A/cm²). Secondary ion mass spectroscopy (SIMS) measurements indicate that this notable improvement in device characteristics stems from reduced diffusion of oxygen, rather than indium, from the ITO into the a-Si:H layer, thus, preserving the integrity of the Schottky interface [8].

The shift in leakage current of the photodiode is measured to be insignificant at low reverse voltages. For example, the shift stabilizes to a value less than 9% when biased at −2 V (see Fig. 7). Even at high reverse voltages (Vₚₑᵥ = −10 V), the dark current increases by no more than a factor of 3; its value being smaller than that observed in Mo/a-Si:H Schottky diodes [9]. Further improvement of both dark and photocurrent has been shown possible by introducing a thin a-SiN insulator film between a-Si:H and ITO layers [10].

The spectral response of the photodiode is shown in Fig. 8 for wavelengths in the range of 400–800 nm. As expected, the behavior of photocurrent is governed by the absorption characteristics of a-Si:H. The maximum photocurrent is at 570 nm and the spectral response is well matched to the light emitted from phosphors when subject to X-rays [2].

The detector demonstrated here extends the applications of a-Si:H technology to both optical imaging (e.g. in document scanning) and X-ray imaging. In particular, with the latter, the low temperature ITO process reported here enables simple co-integration of the scintillating (phosphor) layer for enhanced X-ray conversion efficiency.

The phosphor material considered in the current study is terbium-doped gadolinium oxysulphide (Gd₂O₂S:Tb),
which converts X-ray photons to green light. For high conversion efficiency, highly dense phosphor films need to be uniformly coated on the entire surface of array. However, due to the complex chemistry, the challenges lie not only in building a multi-phase homogeneous system, allowing solid phosphor powders to thoroughly disperse into a polymer matrix, but also in the deposition process, which should result in defect free films with desirable physical properties. Also, the overall deposition process, including the curing step, must be carried out at low temperature (<100°C) to minimize composite film stress. Keeping these crucial factors in mind, we have recently developed a composite coating material in our laboratory. The material consists of three components: Gd$_2$O$_2$S:Tb, PVA and water. This chemical system offers a number of controllable parameters such as the concentration of individual chemicals, grain size of phosphors, and viscosity of coating solution. A series of phosphor coatings have been fabricated using a wet chemical casting technique under room temperature. Initial evaluation of phosphor coating performance shows that the X-ray absorption and conversion efficiencies are a strong function of coating thickness, grain size and X-ray energy [11,12].

4. Thin film transistors

In large-area imaging arrays, the leakage current in a-Si:H TFTs should be small enough for retention of the charge on the sensor during the OFF-state of the TFT. Also the instability, i.e. the variation in threshold voltage ($\Delta V_T$) after prolonged gate bias, should be low for reliable read out of signal from the sensor. The TFTs used in this work are based on the inverted staggered structure (see Fig. 9). The fabrication details have been reported elsewhere [5].

Fig. 10 shows the transfer characteristics ($I_{DS}$ vs. $V_{GS}$) at different $V_{DS}$. We observe a rapid transition from the OFF to the ON state at a gate voltage of less than 5 V. The OFF current is less than 0.1 pA and the ON/OFF ratio is better than $10^7$. Although not shown, the device exhibits a reasonable square law characteristic ($I_{DS}^2$ varies almost linearly with $V_{GS}$) for gate voltages larger than the threshold voltage. The extracted values of threshold voltage and device field effect mobility, based on a fit to measured data, are approximately 2 V and 1 cm$^2$/(V s), respectively. These values, including those for the OFF current and ON/OFF ratio, are comparable to those reported for TFTs fabricated using state-of-the-art fabrication technologies [13]. The source of leakage current, the associated mechanisms, and their dependence on the a-Si:H layer thickness have been reported earlier [5]. A systematic characterization of TFTs with different i-a-Si:H layer thickness shows that the optimal thickness for low leakage is around 50 nm.

The variation in the threshold voltage (i.e. $V_T$ shift) can be attributed to two mechanisms: carrier injection into the gate insulator and dangling bond formation associated with weak Si–Si bonds in the active a-Si:H layer. Both $V_T$ shift and leakage current are influenced by the composition of the top a-SiN$_x$:H layer [14]. Here, the composition of the top nitride layer was varied using different NH$_3$/SiH$_4$ gas ratios during deposition. Results of the $V_T$ shift, which were measured after application of a positive voltage of 25 V to the bottom gate for durations of 5, 15, 30 and 60 min, are shown in Fig. 11. We observe that the shift in $V_T$ is significant with respect to stress duration as well as nitride composition; the shift is less significant in films deposited at high gas ratio (nitrogen-rich) as compared to their low gas ratio counterparts (silicon-rich).

Fig. 12 shows the transfer characteristics, including leakage current, for the different bias stress durations for films deposited at high ($R = 25$) gas ratios. Here, we observe the usual increase in the (reverse) leakage currents with increasing (negative) gate voltage. Although not shown, this variation in leakage current is much less significant with bias stress compared to TFTs with nitride films deposited at small gas ratios [14]. Thus, our results show that given the desired a-Si:H layer thickness, a nitrogen-rich top nitride ($R \approx 20$) is needed to achieve both small $V_T$ shift as well as low leakage current.

![I–V characteristics of Mo/a-Si:H Schottky diode X-ray detector.](image)
5. Pixel integration issues

A crucial design requirement in large-area imaging is a high fill factor. In an attempt to achieve high fill factor, we stacked the Schottky diode on top of the TFT (Figs. 13 and 14), and compared its performance with the conventional pixel structure commonly used in imaging applications (Fig. 15). In all pixels, the detector is 200 \( \mu \text{m} \times 200 \mu \text{m} \).

When devices are stacked on top of each other as shown in Figs. 13 and 14, the intrinsic stress of films becomes an important fabrication issue. When a thick Mo layer is deposited on the stacked pixel structure, the layers beneath are unable to withstand the shear stress, causing the films to crack and peel off the substrate (see Fig. 16). Studies regarding film stress have been reported in Refs. [15,16] along with stress values and process conditions to minimize the film stress in stacked pixel structures.

An important requirement in terms of pixel performance is a low leakage current. The leakage current of the sensor (see Fig. 3) in the different pixels is the same regardless of configuration. However, the same is not true for the TFTs. Fig. 17 shows that the leakage current in the fully overlapped structure is very high compared to the other designs. In the fully overlapped pixel structure, when the TFT gate voltage is negative, the electrons in the a-Si:H experience an electric field forming a steady parasitic back channel at the a-Si:H/a-SiNx interface, hence, providing a high conducting path from drain to source. This leakage can be reduced by employing thicker dielectric layers or by suitably modifying the detector structure to reduce the vertical electric field at the top interface [17].

The partially overlapped and non-overlapping pixels are exposed to X-rays for 50 ms at various X-ray dose in the range of 20–200 mR. The number of measured electrons range from 3 to 20 million for the partially overlapped pixel (Fig. 18). However, in the non-overlapping pixel structure, because of the different TFT geometry, the charge transfer for the same bias and measurement conditions is reduced.

An alternative way to achieve high fill factor while keeping the non-overlapping pixel structure is to employ a vertical TFT (VTFT) structure [18]. In contrast to the conventional lateral structure, the channel length in the
VTFT is defined by the a-SiNₓ:H layer thickness in a drain-source island, and thus the channel length can be precisely controlled by film thickness. Crucial benefits of this device are not only in high fill factor imaging, but also for high resolution LCD displays.

6. Capacitance extraction for large-area arrays

With the growing need for both high pixel density and operating speed, the parasitic coupling capacitances associated with a-Si:H TFTs become a major concern in realization of large-area a-Si:H electronics. The capacitive coupling due to geometric overlapping between the gate and source/drain electrodes in the TFT (see Fig. 19) can give rise to charge feedthrough, thus, lowering the pixel voltage [19].

To gain insight into the effect of parasitic coupling capacitances on the overall array performance, we need to extract these capacitances in an efficient manner and with a high degree of accuracy. A common analytical tool for capacitance estimation is the parallel-plate formula. However, the suitability of this simple formula is restricted because it relies only on the overlap area and does not take into account the effect of the fringing field or the dielectric media surrounding the conductors. For example, with the parallel-plate formula, a zero overlap area would yield zero capacitance, which is incorrect since there can be non-trivial capacitive coupling due to the fringing field. Therefore, we resort to numerical simulation. From a computational standpoint, the main difficulties in the numerical extraction of capacitance include:

1. The extreme device geometries, in which the ratio of thin film thickness to other physical dimensions (such as the width and length) can well be of the order of 10⁻³.
2. The floating potential of the glass substrate: the substrate now needs to be included as part of the computational domain.
3. Treatment of multi-dielectric media where the electric field is discontinuous across dielectric interfaces.

The extreme geometry of metal lines and active devices, and the presence of the glass substrate require a large number of panels (or mesh elements) to barely resolve the surfaces of the conductors and the interfaces between two dielectric media. This leads to a very large system of equations. Furthermore, treatment of multi-dielectric media necessitates more accurate approximation of the potential.

These difficulties can be problematic and may even be out of reach for numerical methods, which impose exorbitant
memory requirements. However, these concerns can be addressed effectively using the exponential-expansion (EE) based method, which have recently developed for efficient evaluation of the three-dimensional potential field [20].

Among the main features of the EE method are: (i) the memory requirement is independent of the desired degree of accuracy on the potential and (ii) different forms of parallelisms are available for both remotely distributed networks and closely coupled parallel systems. The above features make it possible for accurate large-scale simulation for capacitance extraction in TFTs involving panel count in the range of a few hundred thousand to several million. A comparison of the EE method with other well-known schemes based on multipole expansion is given in Table 2.

We compute the geometric overlap capacitance between the gate and source/drain electrodes of an a-Si:H TFT. The number of panels used to discretize the conductor surfaces and dielectric interfaces is nearly 400,000. The length, width, and thickness of the structure considered (see Fig. 19) in simulations is 100 \( \mu \text{m} \) x 100 \( \mu \text{m} \) x 11.3 \( \mu \text{m} \). Here, only 10 \( \mu \text{m} \) of the glass substrate \( (\varepsilon_r = 5.84) \) (or silicon substrate \( (\varepsilon_r = 11.9) \)) is considered so as to reduce panel count. The respective layer thicknesses and dielectric constants are listed in Table 3. The length of the source and drain regions is 25 \( \mu \text{m} \) while that of the channel \( (L_{ch}) \) is 15 \( \mu \text{m} \). The gate length is varied from 10 to 32 \( \mu \text{m} \), which corresponds to an overlap length \( (L_{ov}) \) from −2 to 9 \( \mu \text{m} \). Here, the negative sign implies no overlap and the associated value denotes the horizontal separation between the gate and the source/drain electrodes.

The values of the geometric overlap capacitance between gate and source are listed in Table 4 for different \( L_{ov} \). These values are obtained from parallel-plate approximation (column 2) and numerical simulation for glass substrate (column 3) and silicon substrate (column 4). From the simulations, we observe that (i) the capacitance is a non-linear function of \( L_{ov} \) and hence, the overlap area (see Fig. 20); (ii) even when \( L_{ov} \leq 0 \), the capacitance is non-trivial; and (iii) the capacitance increases with increasing permittivity of the substrate material (see Table 4).

7. New challenges in thin film imaging technology and recent results

Recently, there has been growing interest in the fabrication of large-area TFT arrays on thin flexible plastic substrates. This stems from the need for lightweight, unbreakable and foldable computer screens or large-area sensor arrays for imaging of non-planar (curved) surfaces. Although there are cost-related advantages with the use of plastic substrates, there are several technological issues that need to be addressed. First of all, the upper working temperature for most plastics does not exceed 160–200°C. This requires the reduction of the deposition temperature for the a-Si:H, a-Si\( \text{N}_x \), and microcrystalline (\( \mu \text{c-Si:H} \)) films down from the conventional 250–300°C. Secondly, due to the reduced thickness and Young’s modulus, the plastic substrate cannot serve as a mechanical support for the multiplayer device structures, whereby bending-induced mechanical stresses, in addition to the internal stress, can cause the
layers to break and peel off. Thus, mechanical stress in single layers as well as in the composite device structure needs to be optimized.

Reducing the deposition temperature in PECVD a-Si:H technology using a SiH₄ source gas causes a decrease of the hydrogen surface diffusion coefficient, which leads to increased polyhydride bonding in the film to yield poor electronic properties [24]. However, a-Si:H films with predominantly monohydride bonding have been deposited at low temperature by use of hydrogen or helium dilution followed by post-deposition annealing at 160°C [25]. More recently, there have been reports of TFT fabrication at 160°C on Kapton HN films [26] and at 110°C on PET [27], showing performance characteristics close to those fabricated at 250–300°C.

We developed a low temperature TFT fabrication process whereby we have optimized the deposition process for a-Si:H and a-SiNx:H films at 120°C with reduced mechanical stress in the structure [28]. Preliminary optimization of the n⁺ μc-Si:H film has been conducted to obtain high conducting films [29]. These films are used at the source and drain to reduce the contact resistance. The Kapton HN films 2mil (51 μm) thick and 3 in. in diameter were used as substrates. Before fabrication, 0.5 μm thick silicon nitride coatings were deposited on both sides of the plastic substrate. This coating offers protection against humidity and liquid chemical agents and serves as a good mechanical support for the devices. Also, since the thermal expansion coefficient of Kapton HN is about one order of magnitude higher than that of silicon nitride, this coating reduces the thermally induced strain.

Unlike the processes used for TFT deposition on glass, dry etching was used for the silicon nitride, a-Si:H and n⁺ layers, and wet etching for the metal layers. The maximum deposition temperature was determined by the photoresist post-bake. The a-Si:H films were deposited from 10% SiH₄ + 90% H₂ gas mixture. For the n⁺ a-Si:H contact layer, a hydrogen-diluted 1% PH₃ + 99% SiH₄ gas mixture was used. Amorphous silicon nitride films were deposited from a SiH₄ + (50% NH₃ + 50% N₂) + He gas mixture.

The current–voltage and transfer characteristics of the TFT are shown in Figs. 21 and 22, respectively. The OFF-current is less than 10⁻¹² A and the ON-current is more than 10⁻⁷ A to yield an ON/OFF current ratio of more than 10⁶. Using a linear approximation, we obtain an effective device mobility, \( \mu_{\text{eff}} \), using a dielectric constant value \( \varepsilon_{\text{SiN}} = 6 \).

![Fig. 16. Damaged films due to high intrinsic film stress.](image1)

![Fig. 17. Leakage currents of TFTs in the different pixel structures.](image2)

![Fig. 18. Measured electrons vs. X-ray dose.](image3)

![Fig. 19. Schematic diagram of an a-Si:H TFT cross-section.](image4)
In terms of the longer term, there are still several issues with this technology that need to be solved. The fabrication temperature needs to be further decreased to permit use of transparent substrates such as MYLAR. Also, further work is needed in low temperature n\textsuperscript{+}μ-Si:H to increase the conductivity, as these layers are needed at the source and drain regions for decreased contact resistance. Finally, we believe that further significant improvements in device performance, and in particular, in the field effect mobility, may be still possible with use of substrates with reduced surface roughness. Work along the above lines is currently in progress at our and other laboratories.

For improved design of TFTs fabricated on plastic or glass substrate, a physically based SPICE model has been developed. The model describes the dependencies of the characteristic parameters of the TFT (i.e. threshold voltage, subthreshold slope, leakage current, etc.) on the geometrical parameters and bias conditions. The physically based model can be used for optimization of the TFT’s geometrical parameters to decrease its leakage current, which is important for the performance of the imaging array [30].

8. Conclusions

One of the key issues lies in reduction of pixel size. We believe this can be achieved using the approaches outlined in Section 4, which discussed stacked pixel architectures. For real time applications such as fluoroscopy where read-out speed is crucial and the input signal is weak, using TFT as an amplifier (active pixel sensor) instead of a switch may yield improved readout and noise performance. Such a system would have to incorporate more than one TFT per pixel. The active pixel sensor array may also provide a solution for dealing with the increasing data line capacitance and resistance as the technology scales to larger digital

Table 2
Multipole expansion (mp) vs. exponential expansion (ee) methods (p and S\textsubscript{app} denote the order of expansion)

<table>
<thead>
<tr>
<th>Method</th>
<th>Multipole expansion</th>
<th>Exponential expansion</th>
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<tbody>
<tr>
<td>Accuracy</td>
<td>1/2\textsuperscript{p}</td>
<td>10\textsuperscript{−2}−10\textsuperscript{−16}</td>
</tr>
<tr>
<td>Time</td>
<td>O(p\textsuperscript{3}N)</td>
<td>O(S\textsubscript{app}\textsuperscript{2}N)</td>
</tr>
<tr>
<td>Memory</td>
<td>O(p\textsuperscript{3}N)</td>
<td>O(N)</td>
</tr>
<tr>
<td>Applications</td>
<td>FASTCAP [22], This work</td>
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Table 3
Thickness (µm) of various layers and their dielectric constants

<table>
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<tr>
<th>Layer</th>
<th>Thickness (µm)</th>
<th>Dielectric Constant</th>
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<tr>
<td>a-SiN\textsubscript{x} (gate)</td>
<td>0.26</td>
<td>4.5</td>
</tr>
<tr>
<td>a-Si:H</td>
<td>0.05</td>
<td>11.9</td>
</tr>
<tr>
<td>a-SiN\textsubscript{x} (top)</td>
<td>0.25</td>
<td>3.1</td>
</tr>
<tr>
<td>Source–drain metal</td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>Gate metal</td>
<td>0.12</td>
<td></td>
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Table 4
Geometric overlap capacitance from parallel-plate approximation and numerical simulation

<table>
<thead>
<tr>
<th>L\textsubscript{ov} (µm)</th>
<th>C\textsubscript{approx} (fF)</th>
<th>C\textsubscript{simulation} (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>–2</td>
<td>6.52</td>
<td>11.0</td>
</tr>
<tr>
<td>–1</td>
<td>8.55</td>
<td>14.5</td>
</tr>
<tr>
<td>0</td>
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<td>23.0</td>
</tr>
<tr>
<td>1</td>
<td>42.7</td>
<td>49.3</td>
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<tr>
<td>2</td>
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<td>76.3</td>
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<td>9</td>
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</table>

Fig. 20. Fringing factor α = C\textsubscript{approx}/C\textsubscript{simulation} as a function of overlap length L\textsubscript{ov}. The substrate is glass.

Fig. 21. Current–voltage characteristics of the TFT at different gate voltages.
imaging array formats. With electronics on flexible substrates, the fabrication temperature needs to be further decreased and optimized for good electronic grade quality of materials (low defect density and low stress). Also further significant improvements in TFT performance, and in particular, in the field effect mobility, may be still possible with use of substrates with reduced surface roughness.

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