Semicond. Sci. Technol. **13** (1998) 1225–1246. Printed in the UK PII: S0268-1242(98)92359-8

TOPICAL REVIEW

# Strained-Si heterostructure field effect transistors

**C K Maiti†, L K Bera and S Chattopadhyay**

Department of Electronics and ECE, IIT, Kharagpur 721302, India

Received 9 March 1998, accepted for publication 14 July 1998

**Abstract.** The purpose of this review article is to report on the recent developments and the performance level achieved in the strained-Si/SiGe material system. In the first part, the technology of the growth of a high-quality strained-Si layer on a relaxed, linear or step-graded SiGe buffer layer is reviewed. Characterization results of strained-Si films obtained with secondary ion mass spectroscopy, Rutherford backscattering spectroscopy, atomic force microscopy, spectroscopic ellipsometry and Raman spectroscopy are presented. Techniques for the determination of bandgap parameters from electrical characterization of metal–oxide–semiconductor (MOS) structures on strained-Si film are discussed.

In the second part, processing issues of strained-Si films in conventional Si technology with low thermal budget are critically reviewed. Thermal and low-temperature microwave plasma oxidation and nitridation of strained-Si layers are discussed. Some recent results on contact metallization of strained-Si using Ti and Pt are presented.

In the last part, device applications of strained Si with special emphasis on heterostructure metal oxide semiconductor field effect transistors and modulation-doped field effect transistors are discussed. Design aspects and simulation results of n- and p-MOS devices with a strained-Si channel are presented. Possible future applications of strained-Si/SiGe in high-performance SiGe CMOS technology are indicated.

## 1. Introduction

In conventional Si technology, complementary metal–oxide–semiconductor (CMOS) structures dominate the integrated circuit market. Their popularity comes from the simplicity in processing as well as their high input impedance. However, the p-channel devices are inferior to the n-channel ones in terms of current drive capability and speed performance. This is a consequence of lower mobility of holes compared with that of electrons in Si. In order to match the current drive capability of n-channel (n-MOS) devices, p-channel (p-MOS) devices are designed about 2–3 times larger than n-MOS devices. This adversely affects the level of integration and device speed. A high mobility in the channel of an MOS field effect transistor (MOSFET) will improve both circuit speed and the level of integration. In order to improve the speed of VLSI–ULSI circuits, new materials and device structures are being proposed. The advances in the growth of strained-silicon (strained-Si) layers on relaxed SiGe buffer layers, combined with higher values of both the hole and the electron mobilities in strained Si, have led to increased interest in silicon-based heterojunction field effect transistors (HFETs) using conventional Si-processing technology.

Heteroepitaxy of semiconductor materials has been an active area of research for the last two decades. The interest is driven by the possibility of creating novel electronic and optical devices, as well as integrating existing devices in different materials systems, leading to the production of integrated circuits with increased functionality and lower cost. The foundation of heteroepitaxy was laid by two important contributions: one by Frank and van der Merwe in 1949 [1] who showed theoretically that, if a lattice-mismatched layer is grown on a thick substrate, the layer will be pseudomorphic provided that the mismatch is small and the thickness of the layer is not large and the other by Shockley who suggested the use of semiconductors of different bandgaps for fabrication of heterostructure devices [2].

The lattice mismatch in the SiGe material system is 4.2%, resulting in a very high misfit and threading dislocation density. Most of the research has concentrated on devices having strained layers with thicknesses below the critical thickness. $Si_{1-x}Ge_x$ strained layer heterostructure devices were fabricated on Si substrates only in the late 1980s. The key features of the growth

† Author to whom correspondence should be addressed. E-mail address: ckm@ece.iitkgp.ernet.in; fax + 91 3222 55303.

and electronic properties of the strained SiGe alloy system and its applications have been described in several excellent reviews and in recent books [3–6].

Strain-induced modification of Si/SiGe films is found to have a significant impact on the band structure and carrier transport. When a thin film with a larger lattice constant (e.g. $Si_{1-x}Ge_x$) is grown on a smaller lattice constant substrate (e.g. silicon), the film retains the in-plane lattice constant of the substrate and is under a biaxially compressive strain. Figure 1 shows the band offset between a strained $Si_{0.7}Ge_{0.3}$ film grown on silicon. This is known as the type I band alignment where the entire band offset occurs in the valence band (figure 1(a)) while the band offset in the conduction band is very small. This type of structure is favourable for hole confinement and has been exploited in several novel heterostructure devices, i.e. buried channel p-MOSFETs, p-channel modulation-doped field effect transistors (p-MODFETs) and heterojunction bipolar transistors (HBTs) (see for example, a recent review by Konig and Daembkes [7]).

Similarly, a smaller lattice constant silicon epilayer will be under biaxial tension when grown on a larger lattice constant relaxed-$Si_{1-x}Ge_x$ substrate. Figure 1(b) shows the band offset for a strained-Si epilayer grown on relaxed $Si_{0.70}Ge_{0.30}$. In this case, a type II band offset occurs and the structure has several advantages over the more common type I band alignment, as a large band offset is obtained in both the conduction and valence bands, relative to the relaxed $Si_{1-x}Ge_x$ layer [8]. This allows both electron and hole confinements in the strained-Si layer, making it useful for both n- and p-type devices for strained-Si/SiGe-based CMOS technology. Since strained Si provides both larger conduction and valence band offsets and does not suffer from alloy scattering (hence mobility degradation) [9], a significant improvement in carrier mobility can be achieved. Strained Si is more difficult to grow than strained $Si_{1-x}Ge_x$, since bulk $Si_{1-x}Ge_x$ substrate is currently not available and, until recently, the growth of relaxed $Si_{1-x}Ge_x$ without forming a large concentration of defects as a result of dislocation was difficult. Recent studies on the incorporation of a small amount of C atoms in the Si/SiGe material system to develop new types of buffer layers with reduced misfit dislocations may be useful [10]. However, the ability to achieve both n-MOS and p-MOS devices using strained Si provides a promising alternative for next-generation high-performance SiGe CMOS technology (see for example a recent review by Schaffler [11] and references therein).

In this article, we review the present status of the growth of strained Si on relaxed SiGe buffer layers on Si using various techniques and applications of strained-Si films in SiGe-based CMOS technology. Only a brief review is given for well-established results, and readers are referred to the original publications for more details. We give a more in-depth discussion of relatively new results: low thermal budget processing of strained Si, design and simulation of strained-Si channel MOSFETs. Recent progress made in terms of integration issues and the future prospects of strained-Si/SiGe-based high-performance HFETs which may be integrated into Si VLSI–ULSI production are discussed.

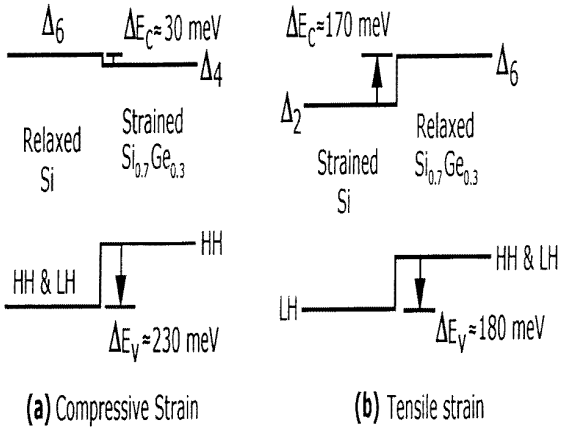



**Figure 1.** Band alignments between Si and $Si_{0.70}Ge_{0.30}$ on two substrates: (a) Si and (b) $Si_{0.70}Ge_{0.30}$.

## 2. Growth and characterization of strained-Si films

Jorke and Herzog were the first to provide experimental evidence for type II band alignment at the interface of an Si/SiGe heterostructure with tetragonal strain distortion in both the layers [12] and Abstreiter and coworkers were the first to introduce the concept of a strain-induced type II band alignment in the Si/SiGe material system [13]. The simplest method of strain adjustment in a buffer layer is to grow a constant-Ge SiGe layer well beyond the critical thickness when a high degree of strain relaxation takes place. Initially, $Si_{1-x}Ge_x$ buffer layers with constant Ge content were grown to a thickness somewhat above the critical thickness for strain relaxation by the formation of misfit dislocations. These were sufficient to demonstrate type II band alignment and electron mobility enhancement by modulation doping in a subsequently deposited Si/SiGe heterostructure with a Si quantum well. This was first reported by Abstreiter *et al* [13] in which a uniform $Si_{1-x}Ge_x$ buffer layer, thicker than the critical thickness, was grown at a high temperature. The strain in the buffer was partially relaxed and a thin Si layer was grown on top of it. The density of threading dislocations introduced as a result of the lattice relaxation was very high and resulted in low electron mobility at 4.2 K.

Despite gradual improvements, the low-temperature mobilities remained behind expectations and one of the main reasons was the known high density ($>10^9$ $cm^{-2}$) of unwanted threading dislocations. It is now known that the problem of high threading dislocation densities in relaxed layers may be avoided by using a series of interfaces with low mismatch and increasing the Ge concentration in steps (step grading) or linearly with a relatively high growth temperature [14–18]. Because of the gradual increase of the lattice mismatch in such a buffer, the misfit dislocation network is distributed over the range of compositional grading rather than being concentrated at the interface with the Si substrate. The greatly improved buffer quality obtained via the compositional grading lowered the threading dislocation density by three orders of magnitude and resulted in a much improved electron mobility at low

temperatures. Strained-layer epitaxial growth on patterned substrates has been attempted [19], which can reduce epilayer threading dislocation densities by up to two order of magnitude. Powell *et al* have proposed a method for producing an almost dislocation-free relaxed SiGe buffer layer on thin SOI substrates. In this growth process, the SiGe epitaxial layer relaxes without the generation of threading dislocations within the SiGe layer; rather, they form in the bottom ultrathin SOI substrate with a superficial silicon thickness less than the SiGe layer thickness [20].

Experimental studies in the last few years on strained SiGe materials have resulted in a significant progress in the understanding of strain relaxation kinetics and optimization of graded buffer layers with respect to relaxation and surface morphology [21–26]. These parameters are of crucial importance as they are interdependent and are affected by growth temperature, grading rate and composition. It appears that the competition between dislocation nucleation and propagation determines the final threading dislocation density in the film. The compositional grading is believed to promote propagation while suppressing nucleation of dislocations and leading to reduced amounts of surface strain, thus allowing higher growth temperatures [27, 28]. In fact, the use of a compositionally graded, relaxed, $Si_{1-x}Ge_x$ buffer layer has been advocated as a 'virtual substrate' and allows the strain in the film to be tailored at will (for a detailed discussion on strain adjustment in SiGe buffer layers, see for example an excellent review by Schaffler [11]).

Many methods exist for the deposition of silicon and $Si_{1-x}Ge_x$ films on silicon at a low temperature. These can be broadly categorized into chemical vapour deposition (CVD) and physical vapour deposition by molecular beam epitaxy (MBE). On the CVD side, Gibbons *et al* at Stanford were one of the first groups to demonstrate high-quality $Si_{1-x}Ge_x$ on silicon. The lamp-heated limited reaction processing reactor (LRPCVD) [29, 30] has been used to grow linearly graded SiGe buffer layers and strained Si. In LRPCVD, the temperature of the wafer is rapidly switched to start and stop the growth process between material layers, and source gases are changed when the wafer is below the growth temperature. Very abrupt interfaces and doping profiles have been achieved by this technique [31]. High-quality, epitaxial, relaxed $Si_{1-x}Ge_x$ layers have been grown by rapid thermal processing chemical vapour deposition (RTCVD) by Jung *et al* [32]. Further improvements of the relaxed buffer (step-graded) layer formation using atmospheric pressure chemical vapour deposition with intermediate *in situ* annealing at high temperature have been reported recently by Kissinger *et al* [33]. Threading dislocation densities as low as 100 $cm^{-2}$ were found, indicating that most of the misfit dislocations really extended throughout the wafer.

The ultrahigh vacuum chemical vapour deposition (UHVCVD) reactor developed at IBM by Meyerson and his coworkers appeared at nearly the same time as LRPCVD. Combining a standard diffusion furnace with ultrahigh vacuum, they have had the most significant impact on the fabrication of $Si/Si_{1-x}Ge_x$ HBTs [14]. The major differences between UHVCVD and MBE techniques, besides the apparatus used, are the silicon and germanium sources used and chamber pressure during growth. High-quality buffer layers have been successfully grown at 550 °C and most of the reported MODFET structures were grown using the UHVCVD technique.

High-quality completely lattice-relaxed SiGe buffer layers have been grown on Si (001) using MBE in the temperature range 750–900 °C and compositional grading on the order of 10% $\mu m^{-1}$ or less with final Ge concentrations of about 30%. Xie *et al* [34] have grown compositionally graded relaxed $Si_{1-x}Ge_x$ buffer layers on Si with various composition gradients and temperatures. The authors reported a threading dislocation density in fully relaxed SiGe buffer layers grown using both MBE and RTCVD in the range $10^5$–$10^6$ $cm^{-2}$ [35]. Gas-source molecular beam epitaxy (GSMBE) [36, 37] has also been successfully employed for the growth of high-quality completely lattice-relaxed step-graded SiGe buffer layers on Si (001) in the temperature range of 750–800 °C. A more abrupt compositional transition of the SiGe/Si interface is expected in GSMBE-grown quantum wells, owing to reduced Ge segregation at the heterointerface [38], than in those grown by solid-source MBE where Ge segregation has been recognized as an important issue [39]. Another advantage of GSMBE is that uniform thickness and composition can be obtained without sample rotation. However, GSMBE is associated with autodoping of doping gas impurities, which would affect the device characteristics.

Structural characterization and determination of film quality of strained layers are usually carried out by transmission electron microscopy (TEM) (both plan view and cross-section) for the determination of defects–dislocations within the layers and measuring the thickness of the layers and by energy-dispersive spectroscopy utilizing a scanning TEM instrument for film composition. Rutherford backscattering spectroscopy (RBS) also yields similar information. High-resolution x-ray diffraction is typically used to determine strain. In this technique, the lattice constant perpendicular to the sample surface, $a_\perp$, is determined. To extract the Ge content and strain state of the film, it is also necessary to find $a_\parallel$. This can be achieved by measuring the Ge content by some other method (e.g. RBS) and $a_\parallel$ can be measured by a grazing incidence x-ray technique. An alternative technique that measures the strain in the film directly is Raman spectroscopy. Sputter depth profiling by secondary ion mass spectroscopy (SIMS) is used to study the chemical composition, e.g. Ge profile. However, this method has a limiting depth resolution of about 3 nm and cannot give a reasonable profile for ultrathin films.

Fitzgerald *et al* [15, 40] have used triple-crystal x-ray diffraction and conventional plan-view and cross-sectional TEM for the determination of strain relaxation. Compositionally graded (10% Ge $\mu m^{-1}$) $Si_{1-x}Ge_x$ films grown at 900 °C by both MBE and RTCVD reveal that for $0.10 < x < 0.53$ the layers are totally relaxed. $Si_{1-x}Ge_x$ cap layers grown on these graded layers are threading dislocation free when examined with plan-view and cross-sectional TEM. Electron beam induced current (EBIC) images were used to count the low threading dislocation

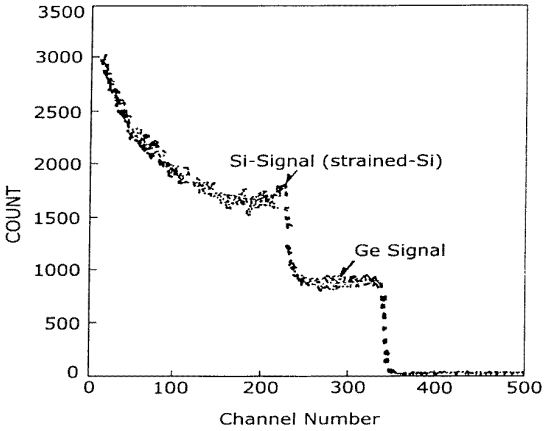



**Figure 2.** RBS spectrum (random) for a strained-Si sample. (After [41].)

densities. The dislocation densities measured by EBIC from MBE-grown samples with final Ge concentrations of 23%, 32% and 50% were found to be $4.4 \times 10^5 \pm 5 \times 10^4$, $1.7 \times 10^6 \pm 1.5 \times 10^5$ and $3.0 \times 10^6 \pm 2 \times 10^6$ cm$^{-2}$, respectively.

To calibrate the $Si_{1-x}Ge_x$ composition in the buffer cap layer RBS is extensively used. Figure 2 shows typical RBS data for a step-graded relaxed $Si_{1-x}Ge_x$ buffer layer together with buffer cap and the strained Si grown using GSMBE [41, 42]. The scattered $He^{2+}$ from the buffer SiGe layer appears at higher energies (channel numbers 250–350) while those from the strained-Si film and from the Si substrate appear at lower energies (channel numbers 50–250). The small peak above the background at the silicon leading edge is attributed to the silicon signal obtained from the top strained-Si layer. The concentration of Ge in the SiGe buffer cap layer and the strained-Si layer thickness are found to be 0.20 and 300 Å, respectively.

Spectroscopic ellipsometry is a non-destructive optical technique which is extremely sensitive to thickness, alloy composition and interfacial conditions of a heterostructure [43]. The pseudo-dielectric function of the sample $\langle\epsilon\rangle$ is obtained from the ellipsometer data and is given by

$$\epsilon = \epsilon_1 + i\epsilon_2. \tag{1}$$

Figure 3 shows the variation of real and imaginary parts of the pseudo-dielectric function with energy for (a) silicon (data used from [44]) and (b) the strained-Si sample. $E_1$ and $E_2$ are the two critical points of transitions and are marked in figure 3. It is observed that there is a shift of the $E_1$ peak, contributed by the strained Si, compared with that of bulk Si. The smaller peak observed at a lower energy (3.1 eV) corresponds to the $E_1$ peak originating from the relaxed uniform-Ge content ($x = 0.18$) $Si_{1-x}Ge_x$ cap layer [41].

The strain state of a relaxed-SiGe buffer layer with a thin strained-Si surface layer may be determined using Raman spectroscopy [45]. A typical scan of a thick $Si_{1-x}Ge_x$ layer with a thin strained-Si layer is shown in figure 4. The peaks in the scan represent resonant phonon modes in the lattice and will depend on both the Ge

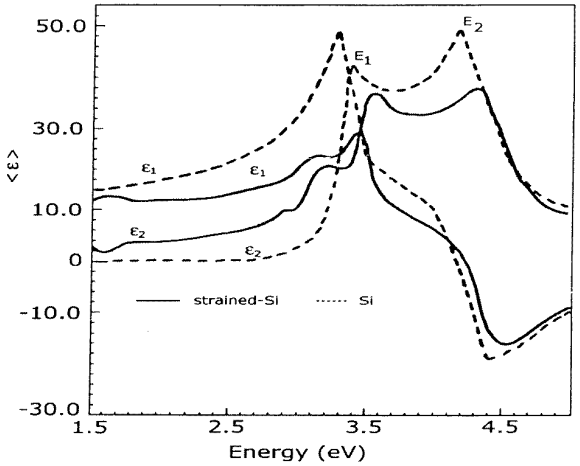



**Figure 3.** Real and imaginary parts of pseudo-dielectric function $\langle\epsilon\rangle = \langle\epsilon_1\rangle + i\langle\epsilon_2\rangle$ for bulk Si (- - - -) and strained Si (——). (After [41].)

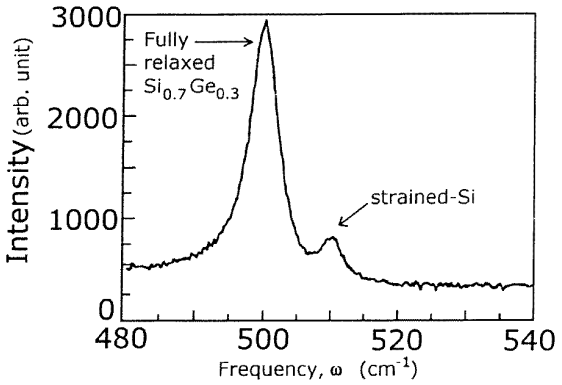



**Figure 4.** High-resolution Raman scan showing Si–Si mode phonon peaks from relaxed-$Si_{0.70}Ge_{0.30}$ layer and strained-Si layer. (After [45].)

content and the strain state of the film. The strain in the film is found from a shift in the wavenumber, $\omega$. Each peak corresponds to a bond between a different pair of atoms, with the two peaks at the lowest wavenumbers (SiGe and Si–Si) originating from the thick $Si_{1-x}Ge_x$ layer and the small peak at the highest wavenumber coming from the thin strained-Si layer.

Semiconductor surface roughness is one of the important parameters which can adversely affect the performance and reliability of the devices. Surface morphology of buffer layers is dependent on the processing conditions such as grading rate and growth temperature. While it has been shown that high growth temperature is desirable for dislocation propagation, it also leads to a 3D growth and eventually a rough surface morphology that may affect lithography steps in subsequent device processing. Atomic force microscopy (AFM) yields information about the surface morphology of a layer. Hsu *et al* have investigated the surface morphology of relaxed, compositionally graded $Si_{1-x}Ge_x$ structures, to illustrate the influence of defect-related strain fields on film growth [25]. Quantitative topographic measurements

via scanning force microscopy show the roughness associated with the cross-hatch patterns oriented along the (110) direction, which basically results from a local accumulation of the underlying misfit dislocations beneath the surface. In addition to AFM, Nomarski optical interference micrographs can also yield similar information about the surface morphology of a relaxed layer [46].

AFM is used for acquisition of highly accurate 3D topographs over an extended scale with a high spatial resolution and the digitized surface topography is represented by a 2D array whose elements express the height information of each point of the 2D-scanned image grid. AFM measurements on GSMBE-grown strained-Si layers have been carried out by Bera *et al* [41] with a model ARIS-3300 instrument (from Burleigh Instruments, Inc.) over a scan region of 3.5 $\mu$m $\times$ 3.5 $\mu$m. Strained-Si films have an RMS surface roughness, an average roughness ($R_a$) and a fractal dimension ($D_f$) of 22.0 Å, 14.6 Å and 2.9, respectively.

## 3. Mobility in strained Si

Optimum semiconductor device design is ultimately based on a full understanding and accurate modelling of charge-carrier transport in semiconductors. Because of its relevance to both basic understanding and device applications, there has always been a strong interest in accurate model descriptions of the mobility as a function of strain, temperature and dopant concentration. For the estimation of maximum theoretical mobilities that can be achieved in modulation-doped Si/SiGe heterostructures and MOSFETs, several theoretical studies incorporating various scattering mechanisms have been reported [47–49]. The main scattering mechanisms to be considered in the strained-Si/SiGe material system are (i) lattice scattering (scattering at acoustic and non-polar optical phonons), (ii) ionized impurity scattering and (iii) neutral impurity scattering. In $Si_{1-x}Ge_x$ materials, alloy scattering becomes important as a fourth independent mechanism [50]. Also, strain distribution in the lattice-mismatched SiGe layer affects the relative importance of intra- and intervalley scattering owing to strain-induced changes in the conduction and valence bands.

### 3.1. Theoretical mobility

Stern and Laux considered remote doping and background doping in the channel as well as the contribution of interface roughness and interface charges. Their results are in good agreement with the experimental data when realistic background acceptor densities between $10^{14}$ and $10^{15}$ cm$^{-3}$ were considered [17, 47, 51, 52]. Monroe and coworkers have studied the limitations of various parameters including scattering from remote dopants, background impurities, interface roughness, alloy fluctuations, strain, morphology and threading dislocations on the mobility [53]. Considering all potential scattering mechanisms which are reasonable, the authors predicted an electron mobility over 1 000 000 cm$^2$ V$^{-1}$ s$^{-1}$, which is comparable with those reached in GaAs/AlGaAs heterostructures.

Several other workers have calculated the expected electron mobility enhancements in strained-Si layers relative to bulk Si [54–58]. Vogelsang and Hofmann [54] have calculated the in-plane electron drift velocities and mobilities in strained Si for 300 K and 77 K. High-field drift velocities were calculated by Monte Carlo (MC) simulations and low-field mobilities by numerical solution of Boltzmann's equation including intra- and intervalley phonon and impurity scattering mechanisms. A mobility enhancement of 74% was obtained at 300 K compared with 36% at 77 K and significant improvements of drift velocities relative to bulk Si up to several 10 kV cm$^{-1}$ were reported. Yamada *et al* [57] have reported an MC study of the low-temperature mobility of electrons. For a device structure having a 10 nm spacer and $2 \times 10^{18}$ cm$^{-3}$ doping, mobility values of $2.5 \times 10^5$ cm$^2$ V$^{-1}$ s$^{-1}$ at 4.2 K and $3.1 \times 10^5$ cm$^2$ V$^{-1}$ s$^{-1}$ at 1.5 K for an electron density of $7.5 \times 10^{11}$ cm$^{-2}$ were obtained. Peak mobility values of $5.0 \times 10^5$ cm$^2$ V$^{-1}$ s$^{-1}$ at 4.2 K and $7.6 \times 10^5$ cm$^2$ V$^{-1}$ s$^{-1}$ at 1.5 K were predicted for wider spacer layer widths and lower channel electron densities. Rashed *et al* [58] have studied the electron transport in the inversion layer of strained-Si channel n-MOSFETs using an MC tool taking into account scattering mechanisms, i.e. phonon, surface roughness and alloy scattering. Table 1 shows the computed low-field electron mobility enhancement factor for strained Si together with some reported experimental device data. For a low level of strain in Si and for low electric fields, electron mobility increases with increasing strain.

High-field velocity saturation and overshoot of electrons in strained-Si channel devices have been studied by Miyata *et al* [56] and the study shows only a slight increase in the saturation velocity at both room temperature and 77 K. As the electric field parallel to the current flow is increased, the drift velocity of the electrons increases and approaches the saturation velocity. These high electric fields are common in short-channel devices, and thus the saturation velocity, rather than low-field mobility, may ultimately limit the performance of scaled devices. The estimated difference between strained- and unstrained-Si saturation velocities is 10% or less [54], and preliminary experimental estimates indicate an enhancement of only 5% [60]. Electron velocity overshoot in strained-Si/$Si_{1-x}Ge_x$ MOSFETs has also been studied using an MC simulator by Gamiz *et al* for steady and non-steady state for high longitudinal field transport regimes [61]. It was concluded that, at high longitudinal fields, the electron velocity overshoot effects, due mainly to the reduction of the intervalley scattering rates as the Ge mole fraction increases, improve MOSFET drain current and transconductance.

The progress in the study of hole mobility in strained Si, however, has been relatively slow. Using strain Hamiltonian and $\boldsymbol{k} \cdot \boldsymbol{p}$ theory, Nayak and Chun [9] have calculated the low-field hole mobility of strained Si. Non-parabolicity and the wrapped nature of the valence bands were included in computation. At room temperature, in-plane hole mobilities were found to be 1103 and 2747 cm$^2$ V$^{-1}$ s$^{-1}$ for Ge contents of 10% and 20% and are 2.4 and 6 times higher than those of bulk Si, respectively.

**Table 1.** Low-field electron mobility: dependence on strain level in Si.

| Ge concentration in the buffer (%) | Strain in Si (%) | Temperature (K) | Mobility enhancement factor | Reference |
|---|---|---|---|---|
| | | | Computed | |
| 10 | 0.4 | 300 | 1.6 | [58] |
| 20 | 0.8 | | 1.8 | |
| 30 | 1.33 | | 1.9 | |
| 2.5 | 0.1 | 300 | 1.14 | [54] |
| 5 | 0.2 | | 1.27 | |
| 10 | 0.4 | | 1.5 | |
| 15 | 0.6 | | 1.65 | |
| 20 | 0.8 | | 1.73 | |
| 25 | 1 | | 1.74 | |
| 2.5 | 0.1 | 77 | 1.28 | |
| 5 | 0.2 | | 1.36 | |
| 10 | 0.4 | | 1.36 | |
| 16.6 | 0.66 | 300 | 2.67 | [56] |
| 33.3 | 1.33 | | 2.67 | |
| 16.6 | 0.66 | 77 | 1.35 | |
| 33.3 | 1.33 | | 1.35 | |
| | | | Experimental | |
| 10 | 0.4 | 300 | 1.45 | [59] |
| 20 | 0.8 | | 1.67 | |
| 29 | 1.3 | | 1.75 | |
| 29 | 1.3 | 77 | 1.35 | |

Table 2 shows the computed low-field hole mobility for strained Si together with some reported experimental hole mobility enhancement factors obtained from device data.

### 3.2. Experimental mobility

Low-temperature Hall mobility measurements are commonly used to determine the overall quality of a heterostructure and are used to optimize the growth parameters. At low temperature, where the thermal effects and scattering by phonons are dramatically reduced, the electron mobility becomes very sensitive to residual scattering mechanisms due to background charge impurities, roughness and dislocation. Experimental electron mobility data from strained-Si/SiGe modulation-doped structures may be divided into two categories: (a) data from devices with the uniform-composition buffer and (b) devices with the compositionally graded buffer. Figure 5 shows the Hall mobility reported by several workers [13, 17, 60, 65–69] using both uniform-composition and graded buffer layers. In the case of the uniform-composition buffer [13, 67, 69], strain relief is a function of buffer layer thickness. In order to achieve a strain level of 1% in Si, which corresponds to a completely relaxed $Si_{0.75}Ge_{0.25}$ buffer, a partially relaxed 0.2 $\mu$m $Si_{0.68}Ge_{0.32}$ uniform-composition buffer is required [71]. For an effective strain level of 1% in Si on a uniform-composition buffer, record high electron mobilities of 1280 $cm^2\ V^{-1}\ s^{-1}$ at 300 K [69] and 17 000 $cm^2\ V^{-1}\ s^{-1}$ at 1.5 K [67] have been reported. In this type of buffer, mobility is limited by the presence of a large number of defects ($10^9$–$10^{10}$ $cm^{-2}$) in the buffer layer. The effect of dislocations on electron mobility has been reported by Ismail. It has been found that the electron mobility is sensitive to threading dislocations when their density exceeds

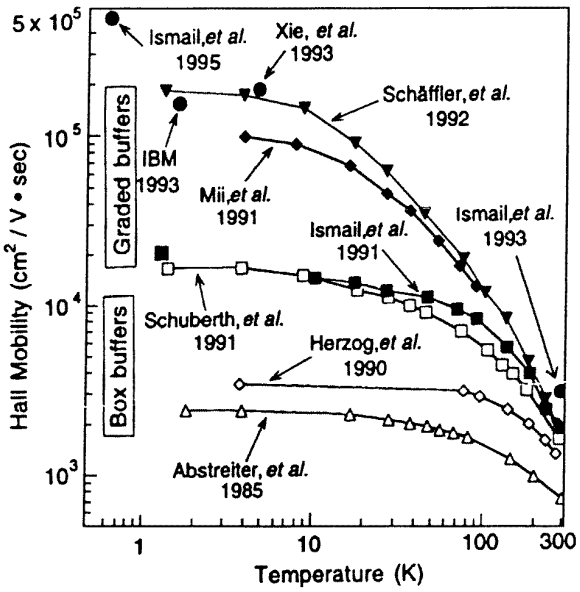



**Figure 5.** Measured electron Hall mobility versus temperature in modulation-doped strained Si. The full symbols are for strained Si grown on high-quality, graded $Si_{1-x}Ge_x$ buffer layers, while the open symbols refer to films with constant Ge content. Data from [13, 17, 60, 65–69] and the plot is after [70].

$3 \times 10^8$ $cm^{-2}$ and decreases by two orders of magnitude when the threading dislocation density is $1 \times 10^{11}$ $cm^{-2}$ [72].

The introduction of graded buffer layers had a great impact on the electron mobility enhancement. The uppermost curve in figure 5 represents very high (around 200 000 $cm^2\ V^{-1}\ s^{-1}$) low-temperature mobilities but

**Table 2.** Low-field hole mobility: dependence on strain level in Si.

| Ge concentration in the buffer (%) | Strain in Si (%) | Temperature (K) | Computed mobility ($cm^2\ V^{-1}\ s^{-1}$) | Reference |
|---|---|---|---|---|
| 10 | 0.4 | 300 | 1100 | [9] |
| 15 | 0.6 | | 1950 | |
| 20 | 0.8 | | 2700 | |
| 25 | 1 | | 3500 | |
| | | | Experimental mobility enhancement factor | |
| 29 | 1.33 | 300 | 1.2 | [62] |
| 18 | 0.8 | 300 | 1.4 | [63] |
| 18 | 0.8 | 77 | 2.0 | |
| 25 | 1.0 | 300 | 1.5 | [64] |

underestimates the 2D electron gas (2DEG) mobility at around room temperature. This is due to parasitic parallel channels of low mobility and unknown carrier concentration in these samples, which freeze out at low temperatures but lead to a reduced average value of the Hall mobility at higher temperatures. By carefully designing the doping concentration in a series of samples, Nelson *et al* [73] could separate the contribution of the 2DEG at room temperature and extracted room-temperature mobilities in excess of 2500 $cm^2\ V^{-1}\ s^{-1}$ for the limiting case of a vanishing parasitic channel. The room-temperature mobility enhancement factor is almost twice that of bulk Si and thrice that of an Si MOSFET. Extremely high electron mobilities obtained in MODFET structures grown using MBE and UHVCVD indicate that similar buffer layer quality has been obtained. By optimizing the MODFET layer sequence and thickness of strained-Si well [74], the best mobility values between 300 000 and 400 000 $cm^2\ V^{-1}\ s^{-1}$ have been obtained. Additional wave functioning by front and back gating of some of the structures led to a record low-temperature (0.4 K) electron mobility in the Si channel of a MODFET beyond 500 000 $cm^2\ V^{-1}\ s^{-1}$ [75, 76], which is an improvement of more than a factor of 10 as compared with the best Si MOSFETs reported.

Room-temperature mobility data are important from device relevance. Typical values are between 2000 and 2800 $cm^2\ V^{-1}\ s^{-1}$ for n channels [60, 77], which exceed those in bulk-Si MOSFETs by a factor of 4–6. High hole mobilities in excess of 9300 $cm^2\ V^{-1}\ s^{-1}$ at 4 K in a p-type modulation-doped $Si/Si_{0.87}Ge_{0.13}/Si$ heterostructure have been reported by Whall and coworkers [78]. For p channels room-temperature values between 1400 and 1800 $cm^2\ V^{-1}\ s^{-1}$ have been reported [79], a factor of 6–9 above those of conventional Si p-MOSFETs.

## 4. Bandstructure of strained Si

The effect of both strain and alloying on the bandgap of strained Si/SiGe material system has been reported in detail by People [8]. In particular, the reported computed conduction and valence band discontinuities have been based on the calculations of van de Walle and Martin [80]. The extracted valence and conduction band offsets between the strained-Si and relaxed-$Si_{1-x}Ge_x$ layers [81] are plotted against theoretically estimated values in figure 6. The extracted values match very well, particularly at low Ge concentration. Substituting the extracted conduction and valence band offset values, the overall bandgap of the strained Si can be obtained and is shown in figure 7 together with the theoretical calculations of People [8].

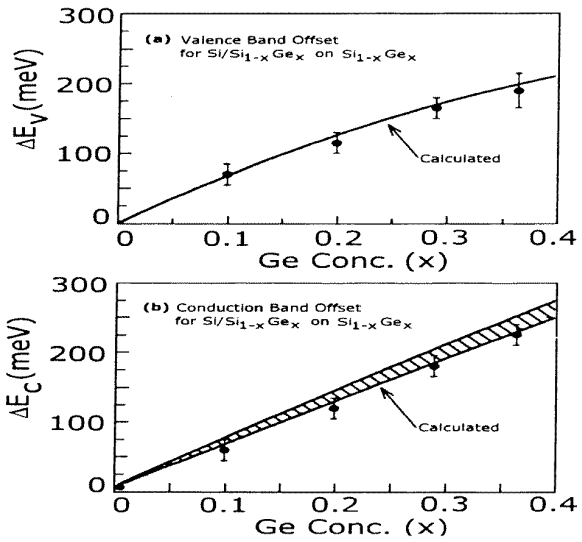



**Figure 6.** Band offsets: (a) valence band and (b) conduction band for strained Si to relaxed $Si_{1-x}Ge_x$. Calculated curves are from People [8] and the data from Braunstein *et al* [81]. Plot is after [45].

The heterojunction band offsets ($\Delta E_c$, $\Delta E_v$) in a strained-Si/SiGe heterostructure have been determined from the measurement of threshold voltages of a surface channel strained-Si p-MOSFET structure (see figure 18(a)) [82]. To determine the threshold voltage at the strained-Si–SiGe interface ($V_{TH}$) and the threshold voltage at the strained-Si–$SiO_2$ interface ($V_{TS}$), the zero-current intercept of the $I_{DS}$–$V_{GS}$ and $I_{DS}$–$g_m^{1/2}$ characteristics were used. The measured values of threshold voltages $V_{TH}$ and $V_{TS}$ were $-1.0$ V and $-1.7$ V, respectively [41, 82]. The extracted experimental valence band offset $\Delta E_v$ was found to be 160 meV. Using the valance band offset value, the conduction band offset was obtained from the following

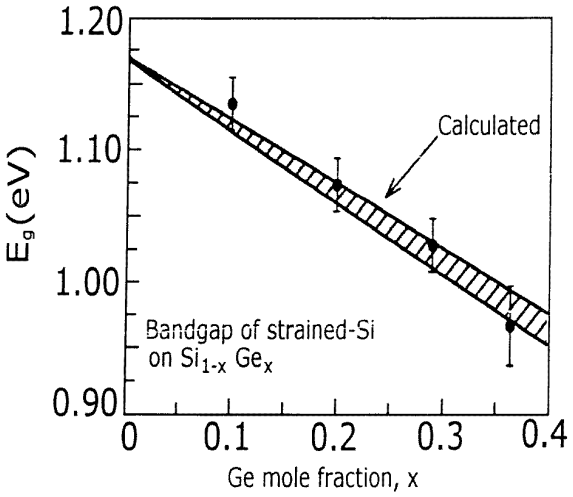



**Figure 7.** Bandgap of strained Si grown on a relaxed-$Si_{1-x}Ge_x$ buffer layer. Calculated curves are from [8] and the data from [81]. Plot is after [45].

equation:

$$\Delta E_c = E_g(\mathrm{Si}_{1-x}\mathrm{Ge}_x) + \Delta E_v(\mathrm{Si}_{1-x}\mathrm{Ge}_x/\mathrm{Si}) - E_g(\text{strained Si}) \quad (2)$$

where $E_g$(strained-Si) is given by [8, 13]

$$E_g = 1.11 - 0.4x \quad (3)$$

where $x$ is the Ge concentration in the top part of a completely relaxed SiGe buffer cap. The conduction band offset $\Delta E_c$ was found to be about 126 meV.

## 5. Oxidation of strained-Si films

High-quality dielectric (oxide or nitride) layer formation is an integral part of MOSFET fabrication. Oxidation of an ultrathin (typically 300 Å) strained-Si layer is a key processing issue as the gate oxide thickness and strained-Si channel thickness (remaining strained Si after oxidation) are determined by this gate oxidation step. High-temperature (>700 °C) processing is not desirable for strained-Si/SiGe structures to prevent strain relaxation and dislocation propagation from the buffer layers. Many of the reported device structures used a MODFET configuration with a Schottky gate to avoid high-temperature gate oxide growth [83–85]. Several workers have used conventional thermal (both dry and wet) oxidation at 750–850 °C for the fabrication of strained-Si MOSFETs [62, 63, 86].

### 5.1. Thermal oxidation of strained-Si films

Device-quality oxides usually result from thermal oxidation of Si. Dry oxygen gas or steam is used at high temperature (typically 800–1000 °C) in the furnace, and the Si reacts with the oxidizing ambient to form $SiO_2$ on the surface of the wafer. During oxidation, Si from the wafer is consumed by the growing oxide, resulting in a loss of approximately $0.44t_{ox}$ of Si for an oxide thickness $t_{ox}$.

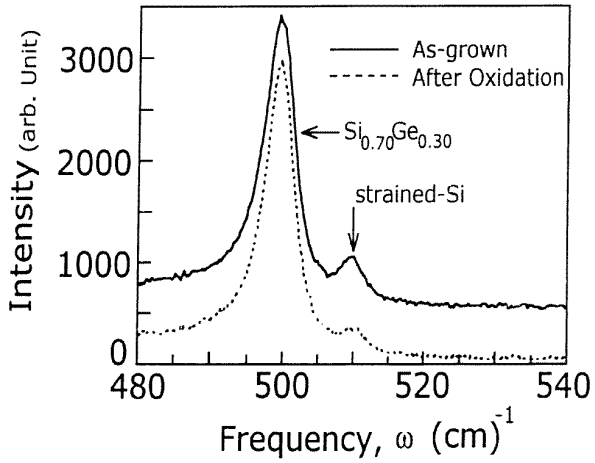



**Figure 8.** High-resolution Raman spectra of a strained-Si layer before and after wet oxidation at 850 °C. (After [46].)

To investigate possible relaxation of strained Si during thermal oxidation, Welser *et al* [46] processed three samples (grown using LRPCVD) with graded $Si_{1-x}Ge_x$ buffer layers ($x = 0.30$), a constant Ge buffer 1 $\mu$m thick and various thicknesses (160, 445 and 1020 Å) of strained Si grown on p substrates. The strained-Si layers were grown at 700 °C and the buffer layers were over 95% relaxed. The samples were p-type doped to $7 \times 10^{16}$ $cm^{-3}$ by flowing 0.5 standard $cm^3$ $min^{-1}$ of diborane during the growth. The samples were oxidized (both dry and wet) at temperatures ranging from 750 to 900 °C in a standard oxidation furnace to yield approximately 13.0 nm of oxide. Figure 8 shows a typical Raman scan before and after oxidation at 850 °C. It is noted that the Si–Si peak size from the strained-Si layer is diminished owing to Si consumption during oxidation, but unaltered peak positions of the Si–Si from the strained Si and buffer $Si_{0.7}Ge_{0.3}$ layer indicate that strain has not been reduced and relaxation remains unchanged in the strained Si and buffer $Si_{0.7}Ge_{0.3}$ layer, respectively.

By measuring the wavenumber shift from the Raman scan for the strained-Si (before and after oxidation) Si–Si line on all of the samples, the strains before and after oxidation were found and are plotted as a function of temperature in figure 9. It is seen that, for all oxidation temperatures, the thinnest strained-Si layer (160 Å) appears to remain fully strained. The 445 Å strained-Si layer is fully strained as grown but shows some evidence of partial strain relaxation during oxidation. Finally, the thickest strained-Si layer (1020 Å) is partially relaxed even as grown and continues to relax more as a function of oxidation temperature.

Since the oxide is relatively thin (≈13.0 nm), the oxide growth rate is expected to be linear and precisely that was reported by Welser *et al* [46]. Figure 10 shows a plot of linear rate constant ($B/A$) for all three strained-Si samples and a control Si sample as a function of temperature. The values extracted for all samples at all temperatures are very similar, well within the expected accuracy of the measurement. In addition, the activation energy for $B/A$ was found to be of the order of 1.7, which is comparable

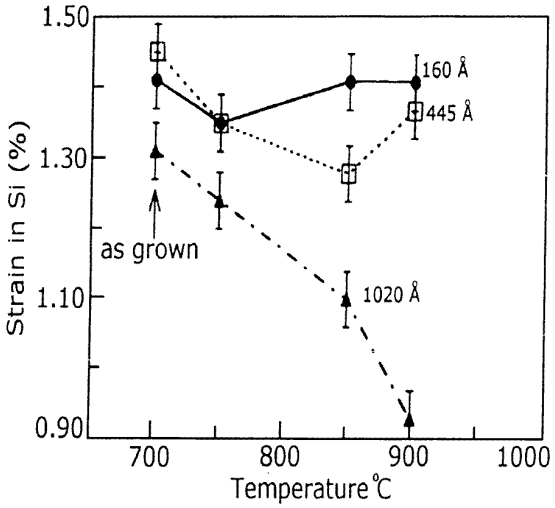



**Figure 9.** Strain in Si layers after thermal oxidation. Si thicknesses refer to as-grown thickness, prior to oxide growth. Wet oxidation times were $t$ = 40, 8 and 2.5 min for 750, 850 and 900 °C, respectively. (After [45].)

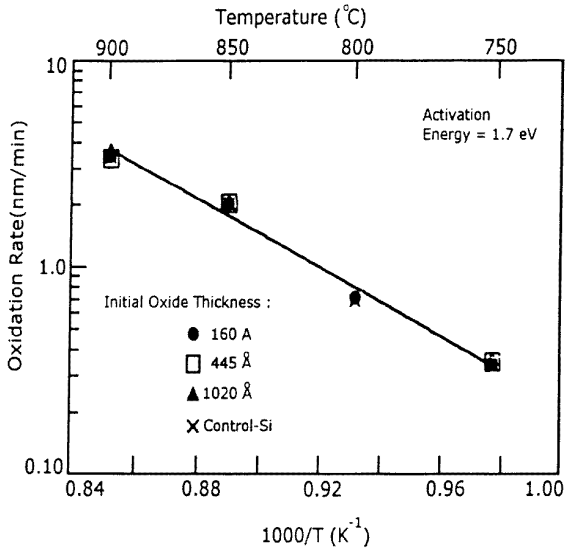



**Figure 10.** Oxide growth rate of strained Si in wet oxidation. The linear rate constant ($B/A$) versus inverse oxidation temperature is plotted. Experiments show very little dependence of oxide growth rate on the initial thicknesses of strained Si. (After [46].)

with the value of 1.96 for bulk Si. Although there was no measured difference between the average growth rate of oxide on strained Si and that on bulk Si, the authors reported that the oxidation rate decreases slightly as the strain in the Si layer increases.

Thermal (dry) oxidation of strained Si (300 Å thick on a fully relaxed step-graded SiGe buffer grown using GSMBE on a p substrate) at 700 °C and quantum hole confinement in accumulation at the strained-Si–SiGe interface has been reported by Bera *et al* [88] as shown in figure 11. The simulated hole confinement in accumulation in an $SiO_2$/strained-Si/SiGe heterostructure using a 1D numerical Poisson solver is also shown. All simulations were

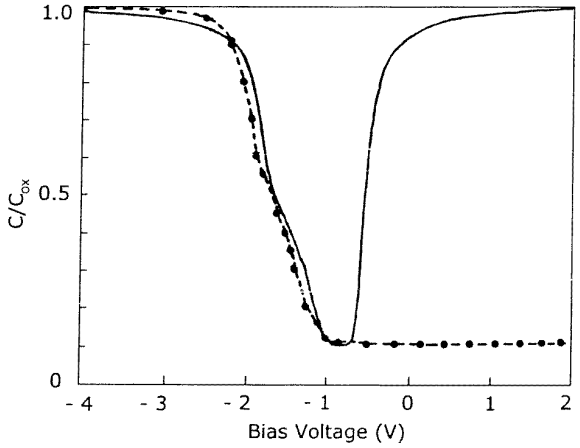



**Figure 11.** $C$–$V$ characteristics of thermally (700 °C, 140 min, dry) grown oxides on strained-Si sample: ●, experimental data; computed low-frequency (——) and computed high-frequency (- - - -) $C$–$V$ plots. (After [88].)

performed for strained-Si/SiGe channel widths exceeding 200 Å, and quantum effects were neglected. At the $SiO_2$–strained-Si interface, a trap density at the middle of the bandgap of $2 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$ was assumed.

### 5.2. Low-temperature oxidation of strained-Si films

As discussed above, there is evidence of oxidation-induced partial strain relaxation in thicker strained-Si films, which continues to increase as a function of oxidation temperature. Low-temperature oxidation of strained-Si/SiGe films is thus important for achieving a high-quality gate oxide while maintaining the pseudomorphic nature of the film. It has also been reported in the literature that the mobility of strained Si degrades owing to the presence of a high fixed oxide charge ($\sim 4 \times 10^{11}$ cm$^{-2}$) [46, 62, 86]. Bera *et al* have reported the growth of ultrathin oxides (<100 Å) on strained-Si layers at a very low temperature (<200 °C) using microwave $N_2O$ plasma and microwave electron cyclotron resonance $O_2$ plasma [87, 88]. The electrical properties of the plasma-grown oxides are shown in table 3. The values of fixed oxide charge density ($Q_f/q$) are found to be lower in plasma-grown oxides than in thermal oxide [46, 62]. However, the interface state densities ($D_{it}$) at mid-gap of the oxide grown using thermal (dry) and microwave $O_2$ plasma are higher than that of microwave $N_2O$ plasma grown oxide. The breakdown field strength of the $N_2O$ plasma grown oxide is comparable with that of the mainstream thermal oxide.

## 6. Nitridation of strained-Si films

In Si, various types of oxynitride processes such as ROXNOX and $N_2O$ treatment have been employed to retard the boron penetration and to improve the oxide integrity [91–94]. For strained-Si-channel MOSFET applications, it is thus important to study the growth of gate-quality oxynitride films on strained Si. However, the growth temperature should be much lower than that of the

**Table 3.** Electrical properties of dielectric films on strained Si.

| Processing condition | Temperature (°C) | $Q_f/q$ ($cm^{-2}$) | $D_{it}$ ($cm^{-2}$ $eV^{-1}$) | Breakdown field (MV $cm^{-1}$) |
|---|---|---|---|---|
| Thermal oxidation | | | | |
| Wet oxidation [45] | 850 | $2.0 \times 10^{11}$ | $(5.5–10)\times10^{10}$ | – |
| Dry oxidation [62] | – | $4.1 \times 10^{11}$ | $1.3 \times 10^{12}$ | – |
| Microwave plasma oxidation | | | | |
| $N_2O$ plasma [87] | 150 | $6.0 \times 10^{10}$ | $1.2 \times 10^{11}$ | 5.0–7 |
| ECR $O_2$ plasma [88] | 150 | $2.6 \times 10^{10}$ | $2.2 \times 10^{12}$ | 2.7–3 |
| Mainstream dry oxidation (Si) [89] | 1000 | $2.5 \times 10^{10}$ | $(1.6–6)\times10^{10}$ | 6–8 |
| Nitridation | | | | |
| $N_2O$+$NH_3$ plasma (2 min + 2 min) [90] | 150 | $6.1 \times 10^{10}$ | $6.5 \times 10^{11}$ | 10–12 |
| $NH_3$ plasma (2 min) [90] | 150 | $6.0 \times 10^{11}$ | $4.7 \times 10^{11}$ | 5–8 |

conventional nitridation or ROXNOX process (typically above 900 °C) to prevent the strain relaxation in strained Si. Bera *et al* [90] have studied the growth and properties of a low-temperature (<200 °C) oxynitride film on strained Si using $N_2O$ and $NH_3$ plasma. Two different types of oxynitride films were grown using a microwave (700 W, 2.45 GHz) plasma cavity discharge system [95]. Table 3 shows the processing condition for various samples. High-resolution x-ray photoelectron spectroscopy (XPS) studies were performed on as-grown and $Ar^+$ ion etched sample surfaces. No nitrogen signal was observed in the XPS spectra from the as-grown film surfaces. Figure 12 shows Si 2p and N 1s photoemission spectra for etched $N_2$ and $N_2O + NH_3$ treated samples. The observed Si 2p peaks are attributed to signals from the Si substrate (∼98.8 eV) and $SiO_xN_y$ layer (around ∼101–103 eV). N 1s spectra of the $N_2O$-grown films exhibit two peaks corresponding to SI≡N bonds at 396.2 eV and $Si_2$=N–O bonds at 400.8 eV. However, the corresponding spectra for $NH_3$-nitrided $N_2O$ oxides show a single peak at 397.9 eV with a higher broadening having a full width at half-maximum of 2.7 eV. The position (397.9 eV) and line shape of the N 1s spectrum in this case suggest that the peak may be a convolution of spectra due to SI≡N, $Si_2$=N–O and Si–N=$H_2$ bonds with the most significant contribution from SI≡N bonds in the sample [96]. It may be noted that the nitrogen atoms accumulate at or near the oxide–substrate interface forming a silicon oxynitride layer. Fixed insulator charge densities ($Q_f/q$) for two samples ($NH_3$ plasma treated and $N_2O$–$NH_3$ plasma treated) are shown in table 3. The minimum value of $Q_f/q$ for the $N_2O$–$NH_3$ plasma treated sample is comparable with that of mainstream thermal oxide ($2.5 \times 10^{10}$ $cm^{-2}$) [97, 98] and shows that a good-quality oxynitride film, necessary for conventional-Si processing technology, is possible on strained Si at a low temperature.

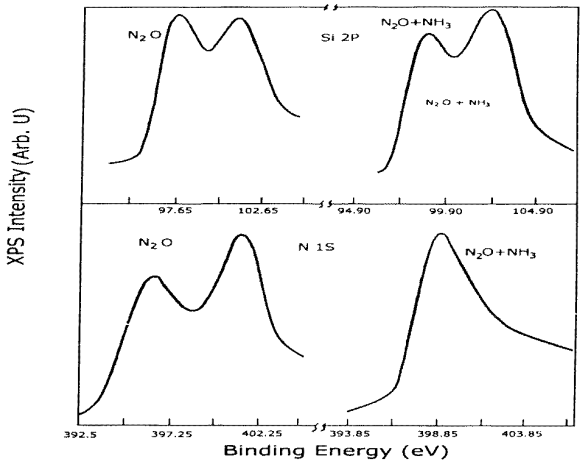



**Figure 12.** High-resolution XPS spectra of Si 2p and N 1s signals after 1 min $Ar^+$ ion etching for $N_2O$ and $N_2O + NH_3$ nitrided oxide on strained Si. (After [90].)

## 7. Contact metallization on strained-Si layers

As both the electron and hole mobilities have been found to be very high compared with those of bulk silicon, strained Si (on a relaxed $Si_{1-x}Ge_x$ buffer layer) has attracted much attention for novel bandgap engineered heterostructure devices. In addition to MOSFETs, many of the reported strained-Si device structures used a MODFET configuration with a metal Schottky gate [84, 85, 99]. Schottky contacts play an important role in the performance of semiconductor devices for various electronic and optoelectronic applications.

Chattopadhyay *et al* have reported the Schottky barrier heights and ideality factors of Pt and Ti on p-type strained Si (grown on a graded relaxed $Si_{0.82}Ge_{0.18}$ buffer layer) in the temperature range 90–300 K using the current–voltage ($I$–$V$) characteristics [100, 101]. It has been found that while the ideality factor decreases with an increase in temperature, the barrier height increases for both the metals. The interface state density of Pt/p-strained-Si Schottky contacts has been determined using experimental forward bias current–voltage ($J$–$V$) and capacitance–voltage ($C$–$V$) techniques. The effects of interfacial oxide layer and series resistance present in the structure have been studied in detail [102].

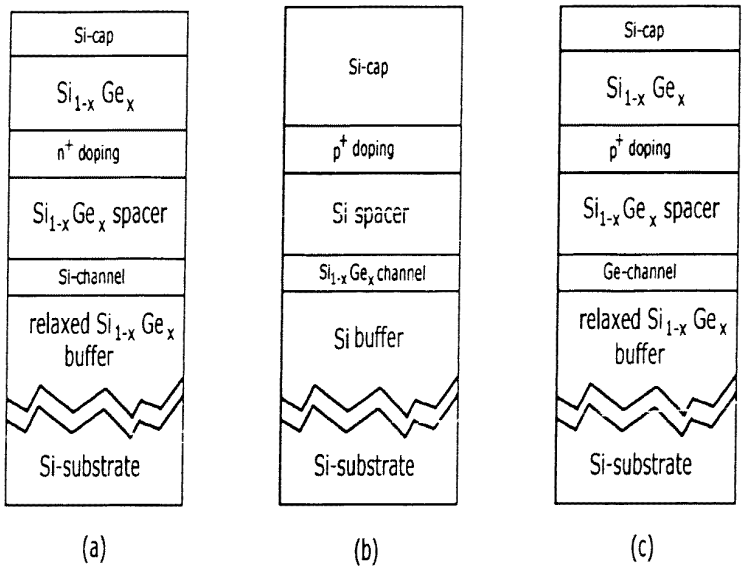



**Figure 13.** Typical layer sequences: (a) n-MODFETs with Si-channel on relaxed-SiGe buffer, (b) p-MODFET with SiGe channel and (c) p-MODFET with Ge channel on relaxed-SiGe buffer. (After [11].)

## 8. Device applications

Si CMOS transistors are the most important building block in digital integrated circuits owing to low power consumption and matured technology. The use of strained Si/SiGe materials promises to improve the speed–power performance of CMOS devices by offering higher electron and hole mobilities. Device applications of strained-Si/SiGe with special emphasis on heterostructure MOSFETs and MODFETs are discussed below.

### 8.1. MODFETs

In a MODFET, carriers are separated from their parent donor or acceptor atoms as they fall across a heterojunction to a lower-energy undoped layer. A typical MODFET structure consists of a thin (5–30 nm) well with quantized states in which the carriers move collision free (2D electron or hole gas (2DEG or 2DHG)), n wells are strained Si [84, 103] or p wells are SiGe (typically up to 30% Ge) [104, 105]. Doping is accommodated in a neighbouring SiGe layer or in an Si layer separated from the well by a thin undoped spacer (2–20 nm). The doped layer can be several nm thin or only a subatomic $\delta$-doped layer. Figure 13 shows the layer sequence typically used for n-MODFETs with an Si channel and graded-SiGe buffer layer. For a detailed discussion on layer sequence and proper design of a MODFET, see [11]. High-quality quantum wells require very complex buffers in order to compensate the large misfit to the Si-substrate, a careful adjustment of the layer sequence and thicknesses, composition and strain states and the doping levels. Extensive experimental work on the modulation-doped structures (mostly n-MODFETs) involving strained Si on relaxed $Si_{1-x}Ge_x$ layers has been performed by several groups [73, 84].

Early work used a uniform-composition buffer, where the Ge content was kept constant, and recent work uses a compositionally graded buffer, where the Ge content is varied. Linear or step grading is essential to minimize dislocation faults and buffer layers have to be thick (3 $\mu$m) for strained-Si channels. Device fabrication steps include in general a low-temperature processing to avoid degradation of the abruptness of the heterointerfaces, mesa etching and a Pt/Ti/Au Schottky gate with a barrier height of about 0.9 eV. The device dc characteristics obtained were well behaved and an extrinsic transconductance of 40 mS mm$^{-1}$ for a gate length of 1.6 $\mu$m was reported [103]. Table 4 summarizes important parameters of some of the n-MODFETs reported in the literature. The dependence of n-MODFET performance on strain in the Si well and quality of SiGe buffer layer at different temperatures is indicated.

When a compositionally graded buffer layer was employed instead, n-MOSFET performance has been dramatically improved with optimized layer design for high transconductance values by minimizing the distance between the 2DEG and the Schottky gate. For 1.2% strain in Si, room-temperature transconductances of 340 mS mm$^{-1}$ for a 1.4 $\mu$m gate length [85], 330 mS mm$^{-1}$ for a 0.25 $\mu$m gate device [84] and 390 mS mm$^{-1}$ for a 0.5 $\mu$m gate device [108] have been obtained. A 2DEG density of (1–3) $\times$ 10$^{12}$ cm$^{-2}$ has been measured in these devices and a room-temperature mobility of 1500 cm$^2$ V$^{-1}$ s$^{-1}$ was reported. At room temperature the highest reported Hall mobility was 2830 cm$^2$ V$^{-1}$ s$^{-1}$ [85]. At 77 K and for 1.2% strain, transconductances of 670 mS mm$^{-1}$ for a 1.4 $\mu$m gate device [85], 600 mS mm$^{-1}$ for a 0.25 $\mu$m gate device [84] and 520 mS mm$^{-1}$ for a 0.5 $\mu$m device [108] have been measured. Ismail *et al* have shown an improved gate design that resulted in a lower leakage at high temperature with a transconductance of 390 mS mm$^{-1}$ at 300 K for a 0.5 $\mu$m device [108]. These values are comparable with those reported for high electron mobility transistors (HEMTs)

**Table 4.** Dependence of n-MODFET performance on strain in Si and quality of SiGe buffer layer at different temperatures.

| Strain in Si channel (%) | Type of SiGe buffer used | Gate length ($\mu$m) | Temperature (K) | Low-field mobility ($cm^2\ V^{-1}\ s^{-1}$) | $g_m$ (mS $mm^{-1}$)[a] | Reference |
|---|---|---|---|---|---|---|
| 1 | Uniform composition $Si_{0.75}Ge_{0.25}$, 0.2 $\mu$m | 1.6 | 300 | 1550 | 40 (E)<br>70 (I) | [103] |
| 1.3 | Uniform composition $Si_{0.68}Ge_{0.32}$, 0.3 $\mu$m; $Si_{0.5}Ge_{0.5}$/Si | 1.4 | 300 | 1090 | 80 (E)<br>88 (I)<br>155 (E) | [106, 107] |
| 1.2 | Compositionally graded $Si_{0.7}Ge_{0.3}$, 1.5 $\mu$m | 1.4 | 300<br>77<br>300<br>300<br>77<br>77 | | 60–72 (E)<br>100–133 (E)<br>340 (E)<br>380 (I)<br>670 (E)<br>800 (I) | [85] |
| 1.2 | Step graded $Si_{0.7}Ge_{0.3}$ (defect density $10^4\ cm^{-2}$) | 0.25 | 300<br>77 | 1500<br>9500 | 330 (E)<br>600 (E) | [84] |
| 1.2 | Step graded $Si_{0.7}Ge_{0.3}$ | 0.5 | 300<br>77 | 2600 | 390 (E)<br>520 (E) | [108] |

[a] E, extrinsic; I, intrinsic.

fabricated in the GaAs system [109]. These results are very encouraging when considering the technology used for the fabrication of these devices.

The first reported p-channel MODFET in strained Si grown on a relaxed SiGe buffer was with a $TiSi_2$ Schottky-barrier gate contact [104]. Transconductances of 2.5 and 3.2 mS $mm^{-1}$ were measured at 300 K for enhancement- and depletion-mode devices, respectively. Recently, Arafa *et al* have reported a very-high-speed p-type SiGe MODFET using an $Si_{1-x}Ge_x$ channel with $x$ around 0.70 and mesa separation with a Ti/Pt/Au Schottky gate. The structure is shown in figure 14, where an inverted layer sequence is used. For the channel, the Ge is graded from $x = 0.70$ to $x = 0.55$ (from bottom to top) to prevent holes from being pulled to the upper heterointerface under negative gate bias. These structures have resulted in hole mobilities of 800–1000 $cm^2\ V^{-1}\ s^{-1}$ at room temperature and of 3300–3500 $cm^2\ V^{-1}\ s^{-1}$ at 77 K. For a gate length of 0.25 $\mu$m, a maximum extrinsic transconductance of 230 mS $mm^{-1}$ was measured. This high transconductance value has led to a unit current gain cut-off frequency ($f_t$) of 24 GHz and a maximum frequency of oscillation ($f_{max}$) of 37 GHz at room temperature [99, 110]. For a gate length of 0.23 $\mu$m, an intrinsic transconductance of 280 mS $mm^{-1}$ has been obtained, which is more than double the value for a silicon p-MOS at the same gate length [111]. The extracted microwave performance of this device yields $f_t$ and $f_{max}$ of about 30 and 45 GHz, respectively. Further improvements are expected in shorter gate length devices and with the introduction of conventional Si technology, especially self-aligned gate techniques for a reduction in gate–source series resistance.

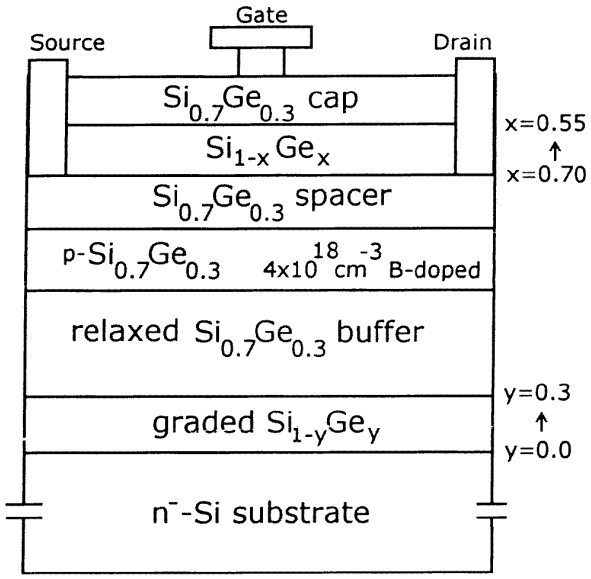



**Figure 14.** Device structure for high-mobility p-MODFET with SiGe channel on relaxed-SiGe buffer. (After [99] ©IEEE 1996.)

### 8.2. Strained-Si-channel n-MOSFETs

Very high electron mobilities demonstrated in strained-Si layers suggest a great potential for this material in high-transconductance n-MOSFETs. To date, in-plane electron mobilities approaching 3000 $cm^2\ V^{-1}\ s^{-1}$ have been reported in long-channel MOSFETs with both surface and buried channels [112]. Figure 15 shows schematic

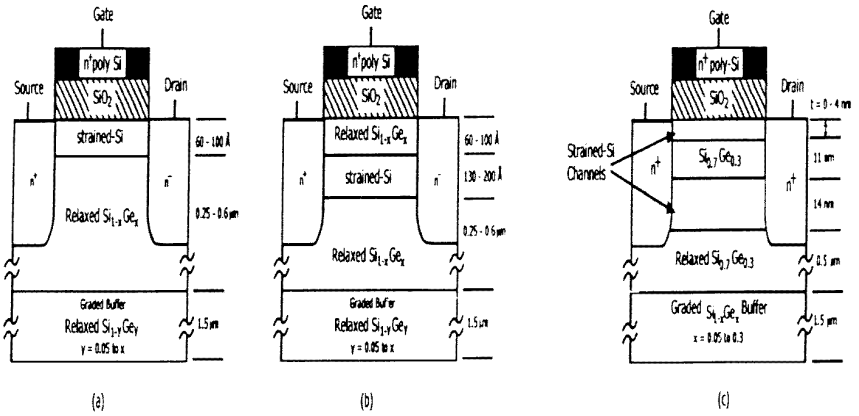



**Figure 15.** Device structures for strained-Si MOSFETs with (a) Si on the surface, (b) Si buried and (c) dual strained-Si channels.

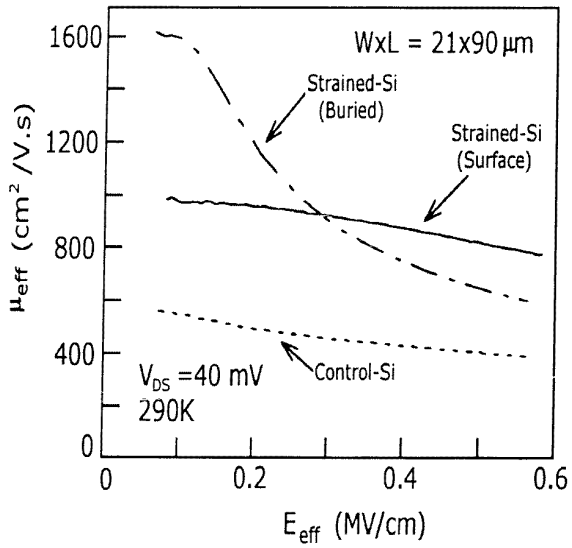



**Figure 16.** Effective low-field mobility versus effective field for different n-MOSFETs. The surface channel strained-Si mobility shows a fairly constant mobility enhancement compared with that of control-Si device, while the buried strained-Si mobility peaks at low fields but decreases rapidly at higher fields. (After [86].)

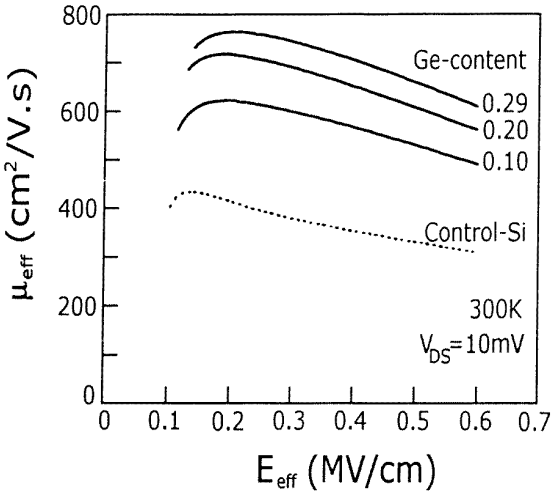



**Figure 17.** Effective mobility of surface channel, strained-Si n-MOSFETs at room temperature. Strained-Si mobility increases with increasing strain (higher Ge content in the relaxed buffer layer). (After [45].)

diagrams of several possible configurations of strained-Si-channel MOSFETs. All the structures have thick, relaxed-$Si_{1-x}Ge_x$ buffer layers, consisting of a layer with linearly graded Ge content followed by a constant Ge content layer. The surface channel device (figure 15(a)) has a single layer of thin strained Si grown on top of the relaxed buffer layer. This layer is oxidized to form gate oxide. The buried strained-Si-channel device (figure 15(b)) has a layer of strained Si buried beneath a thin layer of relaxed $Si_{1-x}Ge_x$. An additional layer of strained Si is necessary to form gate oxide on top of the $Si_{1-x}Ge_x$, but ideally this additional Si layer (sacrificial layer) should be consumed during oxidation. If this sacrificial layer is not consumed fully, then a very thin layer of Si, left between the gate oxide and the $Si_{1-x}Ge_x$ barrier layer (figure 15(c)) which can act as a parallel conducting channel, strongly affects the device performance. Depending on the dopant type in the layers, these structures can be used for n- or p-MOSFETs.

Welser *et al* have fabricated both p- and n-MOSFETs using all these device structures and some of their results on n-MOSFETs are presented below [112, 113]. Long-channel ($L \times W = 10\ \mu\text{m} \times 168\ \mu\text{m}$) surface and buried n-MOSFET devices fabricated on relaxed-$Si_{0.7}Ge_{0.3}$ buffer layers showed well-behaved output characteristics. The effective low-field mobilities for these device structures are shown in figure 16. For the surface channel strained-Si device $\mu_{eff}$ is enhanced compared with the bulk-Si control device and has a similar dependence on the effective electric field. The peak mobility is 1000 $cm^2\ V^{-1}\ s^{-1}$, which shows an 80% enhancement over the Si control (550 $cm^2\ V^{-1}\ s^{-1}$). The peak mobility value for buried channel device is over 1600 $cm^2\ V^{-1}\ s^{-1}$, which is almost 3 times that of the Si control device. Room-temperature effective mobility versus electric field curves of surface channel, strained-Si n-MOSFETs with different Ge contents in the buffer layer are shown in figure 17 together with the

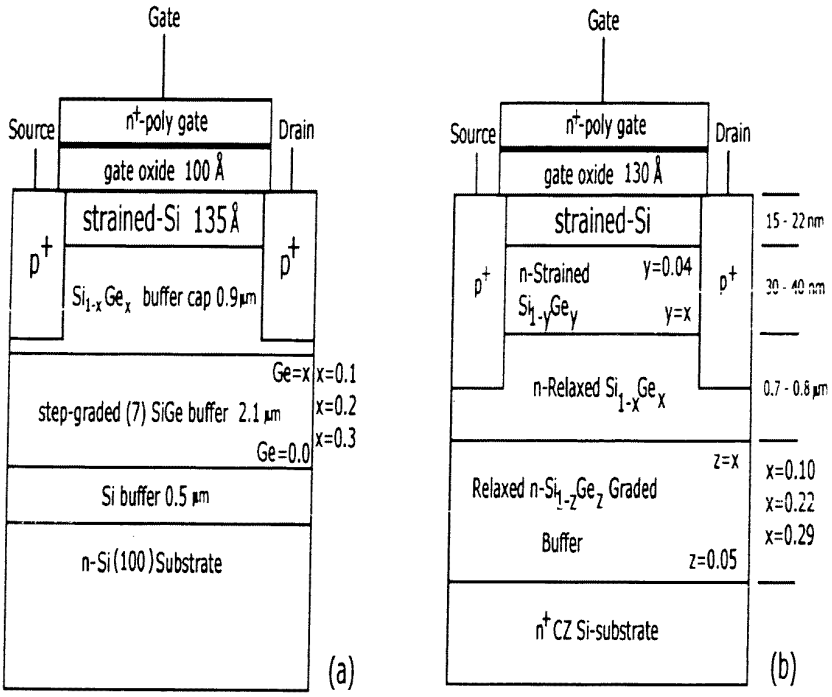



**Figure 18.** Schematic diagram of a strained-Si p-MOSFET: (a) strained Si grown on a fully relaxed SiGe buffer layer (abrupt) and (b) strained Si grown on a grade-back $Si_{1-y}Ge_y$ layer (graded).

mobility extracted from a bulk-Si control device. Strained-Si mobility increases with increasing strain (more Ge content in the relaxed buffer layer) and has little dependence on the effective electric field.

### 8.3. Strained-Si-channel p-MOSFETs

Exploiting the demonstrated higher mobility for 2DHGs, efforts have been made to fabricate strained-Si-channel p-MOSFETs. The aim has always been to improve the speed performance of FETs through the use of heterostructures. Various research groups working on the problem were generally able to achieve better performance with strained-Si compared with control-Si devices. The tensile strain in silicon grown on relaxed SiGe buffer raises the light hole band and lowers the heavy hole band, leading to a significant increase in the low field hole mobility. Observation of hole mobility enhancement in strained-Si p-MOSFETs was first demonstrated by Nayak *et al* [64]. The initial devices were fabricated on a 1 $\mu$m uniform-composition partially relaxed SiGe buffer, which is known to have a very high defect density [15], and this resulted in a limited performance (subthreshold slope 111 mV/decade). Recently, an improved device structure and process to fabricate high-performance strained-Si p-MOSFETs with a high-quality (defect density $<10^5$ cm$^{-2}$) step-graded completely relaxed thick (3 $\mu$m) SiGe buffer layer, a low thermal budget (maximum temperature 700 °C) and a high-quality (100 Å) gate oxide have been reported [63, 82]. The device structure used is shown in figure 18(a). It was shown that the high-field channel mobility of a device with a germanium concentration of 0.18 in the SiGe buffer was 40% and 200% higher at 300 K and 77 K respectively than that of a similarly processed bulk-Si p-MOSFET. This is a consequence of the biaxial tensile strain in Si which improves in-plane hole mobility. Rim *et al* have also reported enhanced hole mobilities in surface-channel p-MOSFETs (see figure 18(b)) employing strained Si on pseudomorphic $Si_{1-y}Ge_y$ on fully relaxed $Si_{1-x}Ge_x$ buffer layers [62].

Figure 19 shows the variation of low $V_{DS}$ ($-0.1$ and $-0.3$ V) transconductances of strained-Si and control-Si p-MOSFETs at 300 K for the device structure shown in figure 18(a). For low $V_{GS}$ the output current is small and remains nearly constant up to $-0.65$ V. The gate voltage at which peak transconductance occurs depends on the value of $V_{DS}$ and the device type, i.e. control Si or strained Si. The control-Si device shows one large peak at $-1.7$ V. However, for the strained-Si devices two peaks are perceptible at $-1.5$ V and $-1.9$ V at 300 K. The peak at $-1.5$ V corresponds to hole confinement at the strained-Si–SiGe buffer interface. At higher gate voltage, however, the holes at the $SiO_2$–strained-Si interface dominate the channel conduction and the device becomes a surface channel device. The transition from buried channel to surface channel is clearly seen from the transconductance plot at 77 K (figure 20). The two peaks ($-1.55$ V and $-2.7$ V) are clearly seen. The $I_{DS}$–$V_{GS}$ characteristics at 77 K for both the strained-Si and the control-Si devices are also shown in this figure. It will be noticed that there is substantial current at $V_{GS}$ close to zero, particularly for the control-Si device. For the strained-Si device the characteristics indicate an accumulation current threshold of about $-1$ V. When the temperature is reduced to 77 K, the mobility improves in

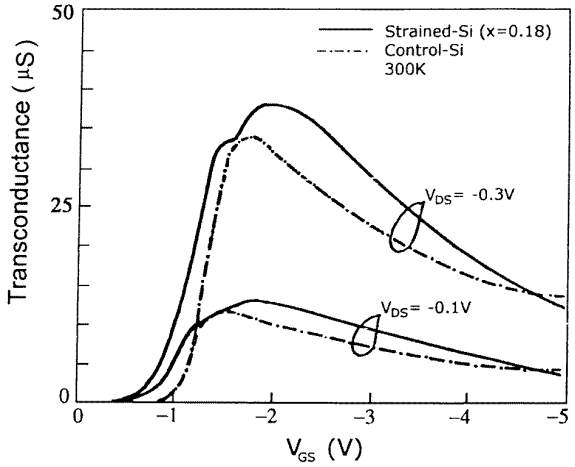



**Figure 19.** Linear transconductances of long-channel ($L \times W$ = 100 $\mu$m $\times$ 300 $\mu$m) strained-Si (on a 18% Ge buffer layer) and control-Si p-MOSFETs at 300 K. (After [82].)

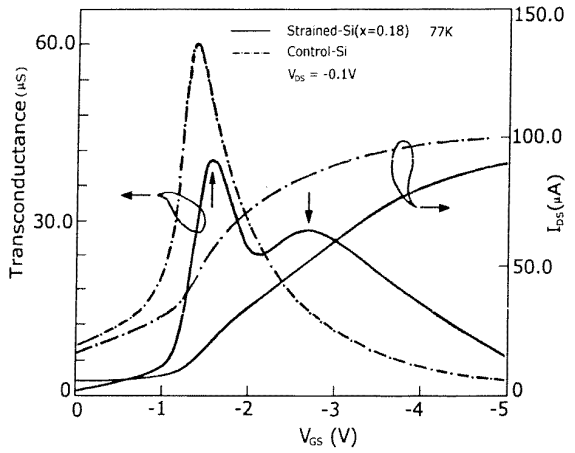



**Figure 20.** Linear transconductances of long-channel ($L \times W$ = 100 $\mu$m $\times$ 300 $\mu$m) strained-Si and control-Si p-MOSFETs at 77 K. Drain currents for the devices are also shown (right-hand scale). (After [82].)

both silicon and strained Si, the factor of improvement depending on the scattering mechanisms operating at the applied gate voltage.

The transverse field dependence of MOS device parameters has assumed a greater importance because of the thinner gate dielectrics and higher doping levels used in submicron MOSFETs, leading to very high transverse electric fields well above 0.5 MV cm$^{-1}$. It is well known that such high fields cause a degradation in device performance. The variation of the effective mobility with electric field is often used as a basis of comparison of MOS devices developed and for computer-aided design. The transconductance factor, field effect mobility and effective mobility computed from $I_{DS}$–$V_{GS}$ characteristics at room temperature and liquid-nitrogen temperature have been compared for strained-Si and control-Si accumulation p-MOSFET devices [82]. Figure 21 shows the variation of computed field effect mobility and effective mobility

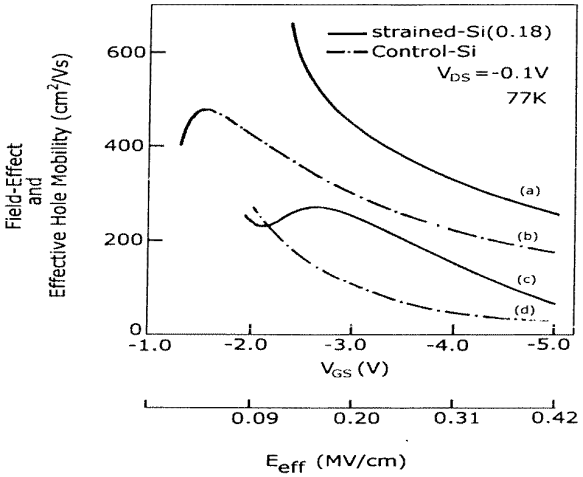



**Figure 21.** Comparison of the field effect and effective hole mobility of long-channel strained-Si and control-Si p-MOSFETs at 77 K: curve a, $\mu_{fe}$ of strained Si; curve b, $\mu_{fe}$ of control Si; curve c, $\mu_{eff}$ of strained Si; and curve d, $\mu_{eff}$ of control Si. The effective electric field values applicable at 77 K for a current threshold value of $-1.0$ V are also indicated. (After [82].)

for strained Si and control Si at 77 K. The effective field values corresponding to the gate voltage (assuming $V_{FB} = -1$ V) are indicated. The presence of the surface and parasitic channel at the strained-Si–$SiO_2$ and SiGe–Si interfaces is indicated by the transconductance (see figure 20). Above $V_{GS} = -2.5$ V, the strained-Si device shows an improvement in both field effect mobility and effective mobility.

### 8.4. Low-frequency noise in strained-Si channel p-MOSFETs

Low-frequency noise is a serious design constraint for critical components in radio-frequency and microwave communication systems as it can lead directly to undesirable spectral broadening. Preliminary results of an experimental study on low-frequency noise in strained-Si and control-Si p-MOSFETs have been reported by Chakrabarti *et al* [114]. The drain current noise of strained-Si devices ($L \times W = 100$ $\mu$m $\times$ 300 $\mu$m) were measured with an EG&G Princeton Applied Research model 5210 lock-in amplifier at various spot frequencies of 1.2 kHz, 12 kHz and 120 kHz and it has been shown that the low-frequency noise of strained-Si p-MOSFETs has a $1/f$ nature and is much lower than that of a bulk-Si device. It has also been noticed that the noise current decreases with the increase in $V_{DS}$ in some ranges. The low-frequency noise spectrum shows evidences of generation–recombination noise [114, 115].

## 9. Simulation of strained-Si-channel MOSFETs

Simulation studies on strained-Si-channel high-performance HFETs have been reported by several workers [116–118]. Abramo *et al* [117] have presented a study on a novel Si/SiGe structure (n-MOSFET) simulated by means of

a one-dimensional quantum mechanical approach which accounts for the quantum nature of the 2DEG. In the simulation, energy splitting between degenerate conduction band valleys of strained-Si layer, optical and elastic acoustic phonon scattering among subbands and surface roughness scattering were implemented. The non-parabolicity effect on the scattering rates and velocities was included by first-order perturbation theory following [119]. Room-temperature low-field peak electron mobility values greater than 2800 $cm^2\ V^{-1}\ s^{-1}$ were predicted. The authors also showed good turn-on characteristics and linear transconductance behaviour for the structure considered.

Although two research groups have demonstrated high-performance strained-Si-channel n- and p-MOSFETs [62, 63, 82, 112], until recently very little information on the design issues has been available in the literature. Careful design considerations are necessary for gate oxide, strained-Si and graded-SiGe layer thicknesses, Ge content and profile and substrate doping required to control the threshold voltage to optimize the device performance. A simulation study of strained-Si short-channel p-MOSFETs has been presented by Armstrong and Maiti [116]. The key design issues for poly-Si contact short-channel strained-Si heterojunction MOSFETs were considered. Analytical models for both electron and hole mobility enhancements in strained-Si and SiGe were used in a 2D device simulator to evaluate the strain dependence of transconductance at both low and room temperature. In case of a p-MOSFET, with the use of a strained grade-back layer, a reduction in valence band discontinuity was obtained at the strained-Si–SiGe interface leading to a significant decrease in hole concentration in the buried parasitic SiGe channel and an increase in transconductance. Simulation results were also verified with experimental device results.

The basic device structures considered for simulation are similar to those shown in figure 18. A 0.8 $\mu$m strained-Si-channel p-MOSFET (figure 18(a), abrupt case) on an $Si_{1-x}Ge_x$ buffer cap (0.9 $\mu$m) grown on top of a step-graded 2.1 $\mu$m relaxed SiGe buffer layer, having a 100 Å gate oxide and a 135 Å thick strained-Si layer, was considered. However, in this structure, a parasitic buried channel is formed at the strained-Si–SiGe interface and leads to device performance degradation owing to lower hole mobility in the relaxed SiGe channel. In the other device structure (figure 18(b), graded case) considered, a thin (300–400 Å) strained graded $Si_{1-y}Ge_y$ buffer cap (grade-back layer) was sandwiched between the strained-Si layer (150 Å) and relaxed $Si_{1-x}Ge_x$ layer (0.7 $\mu$m) to avoid the problem of hole confinement at the strained-Si–SiGe interface as the valence band discontinuity is reduced because of Ge grading. For simulation, a channel length of 0.8 $\mu$m and a 130 Å gate oxide thickness were considered.

To account for the enhanced mobility in both strained-Si and SiGe layers, the low-field hole mobility for $Si_{1-x}Ge_x$ was modelled following [120]. The doping-concentration- and temperature-dependent mobility due to Arora *et al* [121] was modified by using an analytic expression involving Ge content, $x$, as follows:

$$\mu(x, T, N) = \mu_{Arora}(T, N)(1 + 4.31x - 2.28x^2) \qquad (4)$$

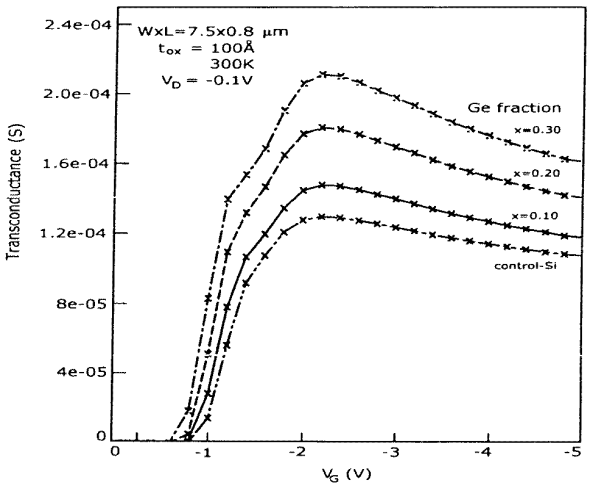



**Figure 22.** Simulated linear transconductance at 300 K ($V_d$ = −0.1 V) for an $n^+$-gate strained-Si p-MOSFET (abrupt case) with various Ge contents ($x$ = 0.10, 0.20 and 0.30) and control-Si device. (After [116].)

and $\mu_{Arora}$ is given by

$$\mu_{Arora}(T, N) = \mu_{1p}\left(\frac{T}{300}\right)^{\alpha_p} + \frac{\mu_{2p}(T/300)^{\beta_p}}{1 + N/N_{cp}(T/300)^{\gamma_p}} \qquad (5)$$

where $\mu_{1p} = 54.3\ cm^2\ V^{-1}\ s^{-1}$, $\mu_{2p} = 407.0\ cm^2\ V^{-1}\ s^{-1}$, $\alpha_p = -0.57$, $\beta_p = -2.23$, $\gamma_p = 2.546$ and $N_{cp} = 2.67 \times 10^{17}\ cm^{-3}$.

Mobility due to alloy scattering is given by [120]

$$(\mu_{alloy})^{-1} = x(1 - x)\ \exp(-7.68x)/124.1 \qquad (6)$$

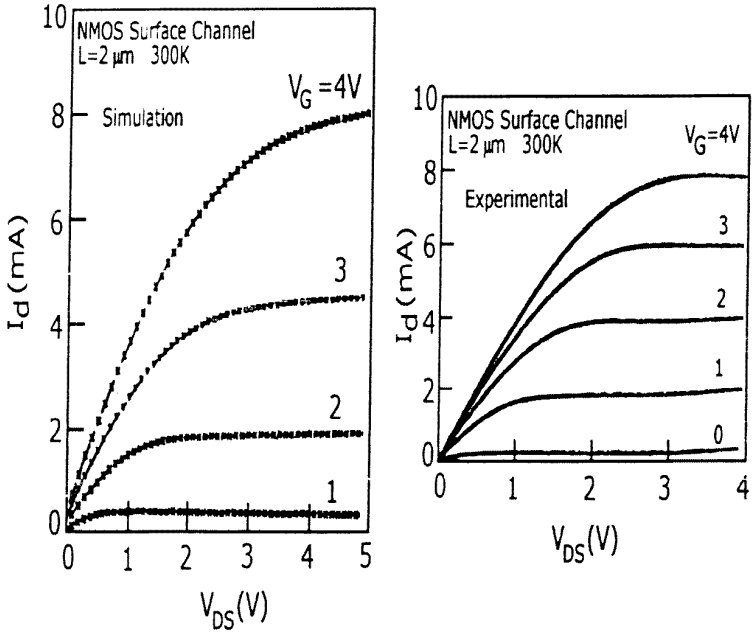
for $x \leq 0.2$ and

$$(\mu_{alloy})^{-1} = \exp(-2.58x)/2150 \qquad (7)$$

for $0.2 < x < 0.6$.

The modified Arora mobility and the mobility due to alloy scattering were combined using Mathiessen's rule and implemented for SiGe regions in a drift diffusion simulator. As the low-field hole mobility in strained Si increases with increasing strain (i.e. with Ge mole fraction, $x$, in the substrate [120]) and because of the absence of alloy scattering in strained Si [9], the enhancement in hole mobility in strained Si was considered to be the same as in SiGe (but without alloy scattering) and was modelled using equation (4). This model was implemented for the strained-Si region through a C interpreter function.

The effect of Ge content on the linear transconductance is shown in figure 22 where the transconductance has been plotted as a function of gate voltage (at $V_d = -0.1$ V) for different Ge content devices. Si device simulation results are also shown for comparison purposes. As seen from figure 22, when compared with a bulk-Si device, a device with an abrupt SiGe cap layer shows a mobility (and hence transconductance) enhancement factor of 1.4 and 1.6 in strained Si for $x = 0.20$ and $x = 0.30$, respectively. The results are comparable with the reported theoretically predicted hole mobility enhancements [63].




(a) (b)

**Figure 23.** Output characteristics of a surface channel strained-Si n-MOSFET: (a) simulated and (b) experimental (data from [113] ©IEEE 1992.)

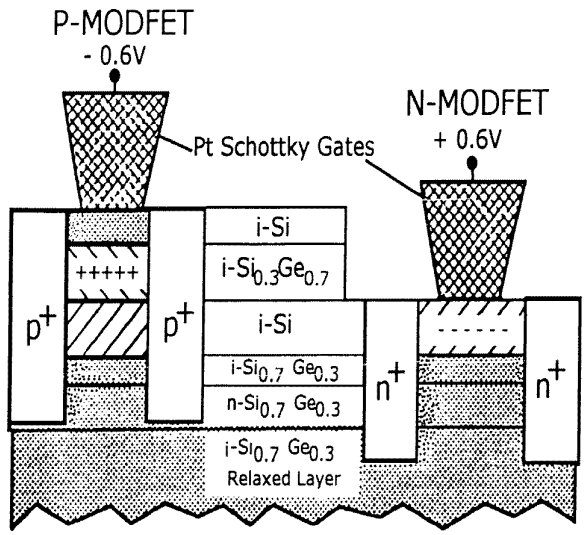



**Figure 24.** Complementary Si/SiGe MODFET cross-section. (After [111] ©IEEE 1995.)

When a grade-back layer is introduced (see figure 18(b)) the problem of confinement of holes at the strained-Si–SiGe interface can be avoided as valence band discontinuity is reduced because of Ge grading. It has been shown that, for a graded cap layer thickness of 400 Å, the discontinuity in the valence band is almost zero and hence confinement of holes and subsequent formation of a parasitic buried channel are reduced and the device becomes a surface-channel one. Agreement with the reported experimental results of Rim *et al* was shown to be good [62]. The authors concluded that the optimal confinement of holes within the strained Si occurs for a graded $Si_{0.7}Ge_{0.3}$ buffer cap thickness of 40 nm and gives rise to an enhancement in transconductance of 30%.

A simulation study of a surface-channel strained-Si n-MOSFET (see figure 15(a) for a typical device structure) has been reported by Armstrong *et al* [118]. An analytical model for electron mobility enhancement in strained Si was used. For simulation, the source and drain region doping of $10^{20}$ cm$^{-3}$ and a junction depth of 0.5 $\mu$m were considered. A channel region doping of $10^{16}$ cm$^{-3}$ was assumed. The fixed oxide charge density was assumed to be $5\times10^{10}$ cm$^{-2}$ and the interface between the strained Si and SiGe is assumed to be defect free. Figure 23(a) shows the simulated output characteristics for a transistor having a gate length of 2 $\mu$m and a width of 7.5 $\mu$m at room temperature for different gate biases. Also shown (in figure 23(b)) are the experimental output characteristics (data reproduced from figure 3(a) in [113]) for a surface channel strained-Si device. A striking similarity between the simulated and experimental data is observed. High electron mobility strained-Si buried n-channel heterostructure MOSFETs (see figure 15(b) for a typical device structure) with a submicron channel length have been investigated by Clifton *et al* using numerical simulation to evaluate the performance [122]. An inversion layer mobility degradation model was included in simulation and a maximum channel mobility of 2600 cm$^2$ V$^{-1}$ s$^{-1}$ were assumed.

## 10. Si/SiGe heterojunction CMOS (HCMOS)

The demonstration of superior performances of both MODFETs and MOSFETs (n and p types) has led to the proposal of combining these device types in analogy to the conventional CMOS. The advantages to be gained by using strained-Si/SiGe in conventional Si CMOS technology have

been examined by several workers [111, 123–126]. As high electron mobility (2200–3000 $cm^2\ V^{-1}\ s^{-1}$) [60] in strained-Si channels under tensile strain and hole mobility (800–1500 $cm^2\ V^{-1}\ s^{-1}$) [127] in compressively strained SiGe channels have been achieved, both n- and p-type MODFETs have been fabricated using both strained-Si and SiGe layers.

For n-MODFETs, the n-doped (phosphorus, 25 keV, $5 \times 10^{14}$ $cm^{-2}$) $Si_{0.7}Ge_{0.3}$ layer is separated from the Si channel by a spacer of 30 Å thick $Si_{0.7}Ge_{0.3}$. The Schottky gate was formed by Pt. These devices demonstrated a large enhancement over bulk Si MOSFETs. The measured peak transconductance at 0.4 $\mu$m gate length was 420 mS $mm^{-1}$, about a factor of 2 higher than in Si n-MOSFETs and comparable with that in GaAs MESFETs or MODFETs at the same gate length. The microwave performance was also impressive. An $f_T$ value of 40 GHz and an $f_{max}$ value of 56 GHz for 0.4 $\mu$m were obtained [111] and are comparable with those of GaAs/AlGaAs HEMTs and may be further improved if an insulating substrate such as SOI is used [20].

For p-MODFETs, the $Si_{0.7}Ge_{0.3}$ layer was doped with boron, followed by a 25 Å thick spacer, and then a strained 40 Å $Si_{0.3}Ge_{0.7}$ channel, which was finally capped with a 200 Å thick $Si_{0.7}Ge_{0.3}$ layer. Schottky contacts were formed using Pt. For these devices, an intrinsic transconductance of 280 mS $mm^{-1}$ at 0.23 $\mu$m gate length was obtained, which is more than double the value for the Si p-MOS at the same gate length. The extracted $f_T$ of 30 GHz and $f_{max}$ of 45 GHz for 0.23 $\mu$m were reported [111] and further improvement is expected as a result of device scaling and use of an insulating substrate such as SOI and advanced processing technology.

Based on the above experimental demonstration, O'Neill and Antoniadis [124, 125] have investigated using computer simulation the high-frequency (microwave) performance of submicron p- and n-channel Si/SiGe-based FETs suitable for CMOS technology. 2D simulation of devices having gate lengths down to 0.1 $\mu$m using a hydrodynamic model demonstrated an enhancement in $f_T$ by around 50% for n-channel devices while it was more than doubled for p-channel devices. Ismail [111] has modelled the performance of Schottky-gate complementary MODFET structures, where electrons would flow through a strained-Si channel and the holes flow through a strained-SiGe layer, both channels being epitaxially grown on Si substrates (see figure 24). For a 0.1 $\mu$m gate length the calculated peak transconductance of the n-MODFET was 820 mS $mm^{-1}$, whereas that of the p-MODFET was 610 mS $mm^{-1}$. The predicted delay for an inverter was 11 ps at a power dissipation per stage of 0.07 mW. Because of inherent problems, such as non-planarity, higher leakage current, difficulty in threshold voltage adjustment and reproducibility for manufacturing associated with Schottky gates, the authors also studied Si/SiGe CMOS structures as shown in figure 25. The structure is planar and uses $SiO_2$ as gate insulator and poly-Si as the gate material. In this case an Si cap layer was used on which either a low-temperature oxide was deposited or gate oxide was thermally grown. For an effective gate length of 0.1 $\mu$m and with an oxide thickness of 50 Å, the predicted transconductances of n- and p-MOSFETs are 750 mS $mm^{-1}$ and 600 mS $mm^{-1}$, respectively. The power–delay product of Si/SiGe CMOS is lower than that of Si-CMOS and SOI technology while operating at a lower supply voltage.

Sadek and his coworkers [123, 126] have proposed a design for an Si/SiGe HCMOS which is planar and avoids inversion of the parasitic surface channel within the designed operating voltage range and presented simulation results demonstrating the feasibility. A schematic cross-section of the proposed structure is shown in figure 26. As discussed above, the design provides for both a compressively strained SiGe hole channel and a tensilely strained Si electron channel in a planar structure. The layers are grown on a low-defect-density ($1 \times 10^5$ $cm^{-2}$) relaxed graded SiGe buffer. The p well is *in situ* doped during growth of the relaxed buffer, while the n well is created by ion implantation prior to growth of the channel layers. An undoped spacer is grown above the well doping in order to adjust the threshold voltage. An n-type $\delta$-doped layer is used to bend the energy bands so as to avoid inversion of the low-mobility Si surface channel. The strained-Si electron channel is separated from the $\delta$-doped layer by an undoped setback layer to minimize ionized impurity scattering. A graded Ge content is used in the strained-SiGe hole channel to minimize the surface roughness scattering by pushing the carriers away from the oxide interface. An Si cap layer is used to grow a high-quality gate oxide. An *in situ* doped $p^+$-poly-Si gate is used for the devices.

Device and circuit simulations show the performance advantage of the proposed technology over bulk-Si CMOS for an effective gate length of 0.2 $\mu$m. Figure 27 shows the simulated power–delay product versus stage delay of an 11-stage inverter ring oscillator, comparing $L_{eff} = 0.2$ $\mu$m Si/SiGe HCMOS with bulk-Si CMOS for unloaded and loaded ($C_L = 10$ fF) cases. The higher carrier mobility of the HCMOS results in a 6.4-fold improvement in power–delay product at a stage delay of 28 ps for the unloaded case and a 4.6-fold improvement at a delay of 55 ps for the loaded case. A minimum delay of 22 ps is predicted for unloaded Si/SiGe HCMOS running at 1.5 V.

Complementary HFETs (CHFETs) can enhance the performance limit of conventional CMOS. Owing to a barrier-confined carrier transport in quantum wells with higher mobility, higher $v_{sat}$ and higher $n_s$ one can expect higher transconductances, higher speed, lower gate delay, lower noise and low power consumption. Because of the enhanced performance of p-HFETs equally sized p- and n-FETs can be designed for higher packing density. Striking performance predictions have been made for SiGe HFETs and Si CMOS. While standard CMOS needs a gate length below 0.2 $\mu$m for transconductances around 400 mS $mm^{-1}$ [128, 129], these are even found at relaxed gate lengths of 1.2–1.4 $\mu$m with HFETs. Sub 0.2 $\mu$m SiGe HFETs will yield more than 800 mS $mm^{-1}$ at room temperature and above 1000 mS $mm^{-1}$ at 77 K [7]. Figure 28 shows the predicted transconductance for HCMOS extrapolated from measurements on 1.2–1.4 $\mu$m MODFETs in comparison with the best Si MOSFETs. These results are corroborated by recent experimental

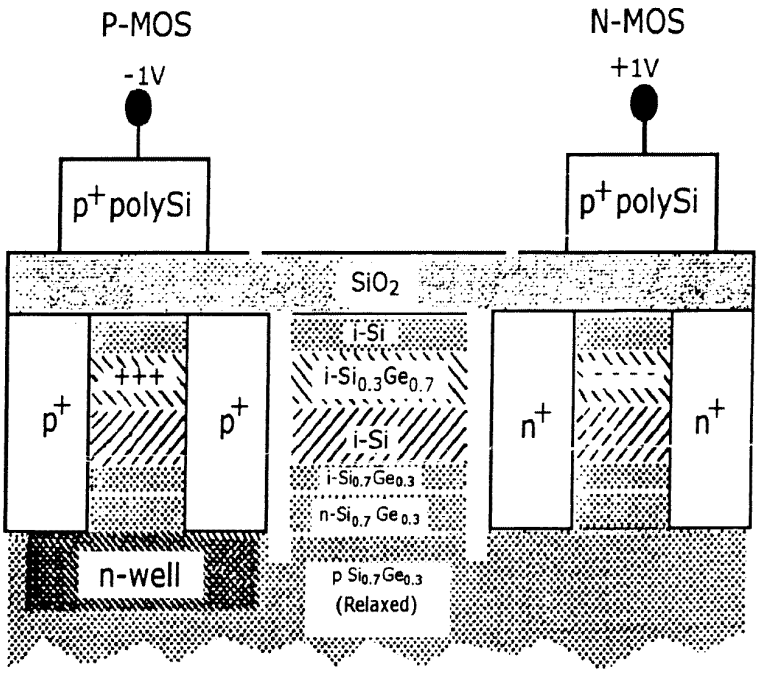



**Figure 25.** Complementary Si/SiGe MOSFET cross-section. (After [111] ©IEEE 1995.)

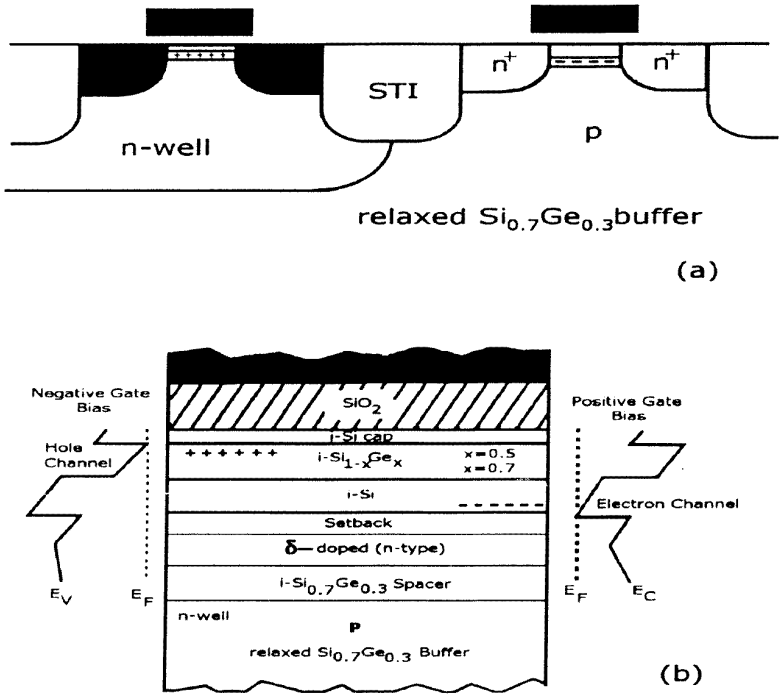



**Figure 26.** (a) Cross-section of a proposed Si/SiGe HCMOS technology device and (b) schematic of channel layers and conduction and valence band for gate bias just above $V_T$. (After [126] ©IEEE 1995.)

demonstrations [111, 130], which are both based on *S*-parameter measurements on mesa-type devices with submicron gates defined by electron beam lithography.

Concerning high-frequency performance of Si/SiGe-HFETs, so far only predictions can be made on the basis of transconductances and gate–source capacitances. The cutoff frequency, $f_t$, at which the current gain falls to unity is defined by

$$f_t = \frac{g_m}{2\pi C_{gg}} \tag{8}$$

where $C_{gg} = \mathrm{d}Q_g/\mathrm{d}V_{gs}$ and $Q_g$ is the gate charge. Recent record sub 0.15 $\mu$m CMOS values have set a new

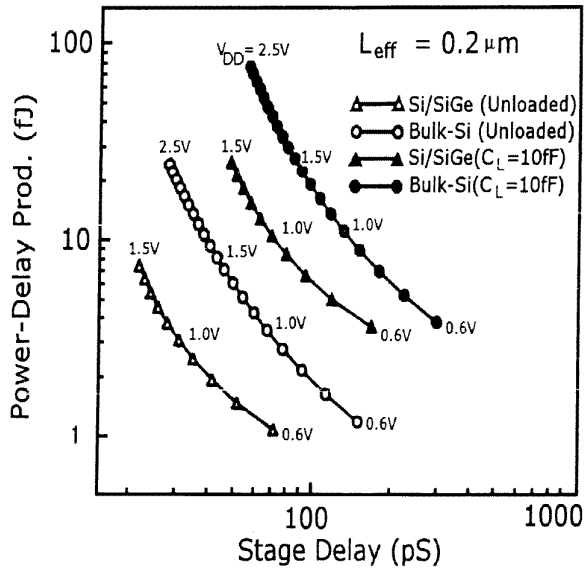



**Figure 27.** Power–delay product versus stage delay for Si/SiGe HCMOS and bulk-Si CMOS. The corresponding drain bias values are indicated on the curves. (After [126] ©IEEE 1995.)

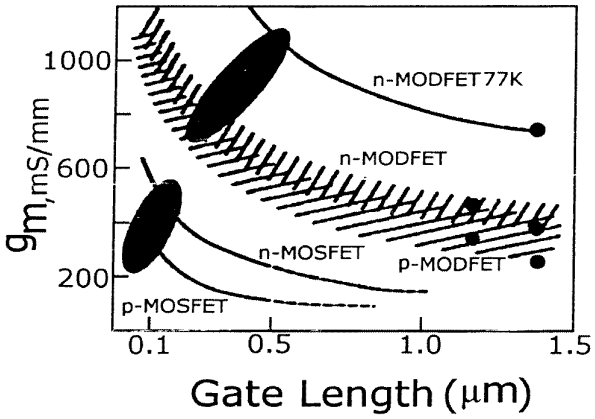



**Figure 28.** Predicted transconductance of high-performance HCMOS extrapolated from measurements on 1.2–1.4 $\mu$m MODFETs, in comparison with best Si-MOSFETs. (After [7].)

landmark [129]. n-MOSFETs have reached 70–118 GHz with gate lengths of 140–90 nm and p-MOSFETs have reached 38–67 GHz between 100 and 65 nm. Simulation predicts beyond 200 GHz for HFETs, perhaps higher, if one can profit from the more pronounced velocity overshoot expected from strained-Si/SiGe [56]. This outstanding performance also has positive consequences for the gate delay. SiGe HCMOS will open the sub 10 ps range for digital applications (see figure 27). It may go down to 2–3 ps, an improvement by factors of 3–5 over the best CMOS values of 11.8–22 ps [128, 129].

The success of n-MODFETs structures grown on graded SiGe buffers with Ge content exceeding 30% suggested an extension to higher Ge contents (up to 100%) to allow p-type structures (Ge/SiGe/Si) with a pure Ge channel and these have been demonstrated [131]. These devices show outstanding Hall hole mobilities at room temperature (up to 1300 $cm^2\ V^{-1}\ s^{-1}$) and 77 K (up to 14 000 $cm^2\ V^{-1}\ s^{-1}$) and the compatibility with Si substrates. The implementation of n- and p-MODFETs is a prerequisite for complementary transistors (CMODFETs) with matched characteristics which cannot be realized in any of the established material systems because of the far inferior properties of the corresponding p-type devices. With almost identical mobilities of electrons in Si and holes in Ge, the Ge/SiGe/Si heterostructures could provide such matched transistor pairs, and moreover, remain compatible with Si VLSI technology. Demonstration of CMODFETs is already under way using a simplified double-mesa structure with a layer sequence consisting of a pseudomorphic SiGe-channel p-MODFET underneath a relaxed SiGe buffer and an n-MODFET structure grown on top of it. This development will require more refined integration concepts and process steps and could open the field of high-speed applications for the complementary logic [70].

## 11. Conclusion

In this paper, a review of recent progress in strained Si on relaxed SiGe technology has been given. Progress in design and fabrication of high-mobility n- and p-channel strained-Si/SiGe devices (MOSFETs and MODFETs) was presented as well as some of the materials and processing issues related to the fabrication of these heterostructures. In addition, an outlook on the integration issues of these devices with CMOS based on Si was presented. Because of their compatibility with conventional Si-processing technology, mobility-enhanced HFETs are expected to provide the performance advantage when downscaling in device dimensions will no longer be possible in bulk Si. Since low-power mixed-mode circuits are becoming increasingly important for mobile communications, Si/SiGe HCMOS technology will be useful for the improvement of high-frequency performance. However, from a manufacturing point of view, several issues of concern are device isolation, interconnects and reliability, which need further experimental investigation in order to assess the potential of Si/SiGe HCMOS.

## References

[1] Frank F C and van der Merwe J H 1949 *Proc. R. Soc.* A **198** 216
[2] Shockley W 1951 *US Patent 2569347*
[3] Bean J C 1992 *Proc. IEEE* **80** 571
[4] Metzger R A 1995 *Comp. Semicond.* **1** 21
[5] Morkoc H, Sverdlov B and Gao G-B 1993 *Proc. IEEE* **81** 493
[6] Jain S C 1994 *Germanium–Silicon Strained Layers and Heterostructures* (New York: Academic)
[7] Konig U and Daembkes H 1995 *Solid-State Electron.* **38** 1595
[8] People R 1986 *IEEE J. Quantum Electron.* **22** 1696
[9] Nayak D K and Chun S K 1994 *Appl. Phys. Lett.* **64** 2514
[10] Jain S C, Osten H J, Dietrich B and Rucker H 1995 *Semicond. Sci. Technol.* **10** 1289
[11] Schaffler F 1997 *Semicond. Sci. Technol.* **12** 1515

[12] Jorke H and Herzog H J 1985 *Proc. 1st Symp. on Silicon MBE Symp. Proc.* vol 85–7, ed J C Bean (Pennington, NJ: Electrochemical Society) p 194
[13] Abstreiter G, Brugger H, Wolf T, Jorke H and Herzog H J 1985 *Phys. Rev. Lett.* **54** 2441
[14] Meyerson B S, Uram K J and LeGoues F K 1988 *Appl. Phys. Lett.* **53** 2555
[15] Fitzgerald E A, Xie Y-H, Green M L, Brasen D, Kortan A R, Michel J, Mii Y-J and Weir B E 1991 *Appl. Phys. Lett.* **59** 811
[16] LeGoues F K, Meyerson B S and Morar J F 1991 *Phys. Rev. Lett.* **66** 2903
[17] Schaffler F, Tobben D, Herzog H J, Abstreiter G and Hollander B 1992 *Semicond. Sci. Technol.* **7** 260
[18] Xie Y H, Fitzgerald E A, Silverman P J, Kortan A R and Weir B E 1992 *Mater. Sci. Eng.* B **14** 332
[19] Hull R, Bean J C, Higashi G S, Green M L, Peticolas L, Bahnck D and Brasen D 1992 *Appl. Phys. Lett.* **60** 1468
[20] Powell A R, Iyer S S and LeGoues F K 1994 *Appl. Phys. Lett.* **64** 1856
[21] LeGoues F K, Mooney M M and Chu J O 1993 *Appl. Phys. Lett.* **62** 140
[22] LeGoues F K, Meyerson B S, Morar J F and Kirchner P D 1992 *J. Appl. Phys.* **71** 4230
[23] Mooney P M, Jordan-Sweet J L, Ismail K, Chu J O, Feenstra R M and LeGoues F K 1995 *Appl. Phys. Lett.* **67** 2373
[24] Hohnisch M, Herzog H J and Schaffler F 1995 *J. Crystal Growth* **157** 126
[25] Hsu J W P, Fitzgerald E A, Xie Y H, Silverman P J and Cardillo M J 1992 *Appl. Phys. Lett.* **61** 1293
[26] Lutz M A, Feenstra R M, LeGoues F K, Mooney P M and Chu J O 1995 *Appl. Phys. Lett.* **66** 724
[27] Li J H, Koppensteiner E, Bauer G, Hohnisch M, Herzog H J and Schaffler F 1995 *Appl. Phys. Lett.* **67** 223
[28] Mooney P M, Jordan-Sweet J L, Chu J O and LeGoues F K 1995 *Appl. Phys. Lett.* **66** 3642
[29] Gibbons J F, Gronet C M and Willams K E 1985 *Appl. Phys. Lett.* **47** 721
[30] Hoyt J L, King C A, Noble D B, Gronet C M, Gibbons J F, Scott M P, Laderman S S, Rosner S J, Nauka K, Turner J and Kamins T I 1990 *Thin Solid Films* **184** 93
[31] Gronet C M, King C A, Opyd W, Gibbons J F, Wilson S D and Hull R 1987 *J. Appl. Phys.* **61** 2407
[32] Jung K H, Kim Y M and Kwong D L 1990 *Appl. Phys. Lett.* **56** 1775
[33] Kissinger G, Morgenstern T, Morgenstern G and Richter H 1995 *Appl. Phys. Lett.* **66** 2083
[34] Xie Y H, Fitzgerald E A, Monroe D, Watson G P and Silverman P J 1994 *Japan. J. Appl. Phys.* **33** 2372
[35] Fitzgerald E A, Xie Y H, Monroe D, Silverman P J, Kuo J M, Kortan A R, Thiel F A and Weir B E 1992 *J. Vac. Sci. Technol.* B **10** 1807
[36] Nayak D K, Usami N, Sunamura H, Fukatsu S and Shiraki Y 1993 *Japan. J. Appl. Phys.* **32** L1391
[37] Nayak D K, Usami N, Fukatsu S and Shiraki Y 1993 *Appl. Phys. Lett.* **63** 3509
[38] Fukatsu S, Yoshida H, Fujiwara A, Takahashi Y and Shiraki Y 1992 *Appl. Phys. Lett.* **61** 804
[39] Kato Y, Fukatsu S and Shiraki Y 1995 *J. Vac. Sci. Technol.* B **13** 111
[40] Fitzgerald E A, Xie Y H, Brasen D, Green M L, Michel J, Freeland P E and Weir B E 1990 *J. Electron. Mater.* **19** 949
[41] Bera L K, Ray S K, Nayak D K, Usami N, Shiraki Y and Maiti C K unpublished
[42] Bera L K, Ray S K, Nayak D K, Usami N, Shiraki Y and Maiti C K 1998 *Proc. Int. Conf. on Computers and Devices for Communication, (CODEC-98)* (Calcutta) p 503
[43] Humlicek J, Garriga M, Alonso M I and Cardona M 1989 *J. Appl. Phys.* **65** 2827
[44] Humlicek J 1995 *Properties of Strained and Relaxed Silicon Germanium* ed E Kasper (London: INSPEC) p 121
[45] Welser J J 1994 The application of strained-silicon/relaxed-silicon germanium heterostructures to metal-oxide-semiconductor field-effect transistors *PhD Thesis* Stanford University
[46] Welser J, Hoyt J L and Gibbons J F 1994 *Japan. J. Appl. Phys.* **33** 2419
[47] Stern F and Laux S E 1992 *Appl. Phys. Lett.* **61** 1110
[48] Fischetti M V and Laux S E 1996 *J. Appl. Phys.* **80** 2234
[49] Takagi S, Hoyt J L, Welser J J and Gibbons J F 1996 *J. Appl. Phys.* **80** 1567
[50] Kay L E and Tang T W 1991 *J. Appl. Phys.* **70** 1483
[51] Nelson S F, Ismail K, Nocera J J, Fang F F, Mendez E E, Chu J O and Meyerson B S 1992 *Appl. Phys. Lett.* **61** 64
[52] Tobben D, Schaffler F, Zrenner A and Abstreiter G 1992 *Phys. Rev.* B **46** 4344
[53] Monroe D, Xie Y H, Fitzgerald E A, Silverman P J and Watson G P 1993 *J. Vac. Sci. Technol.* B **11** 1731
[54] Vogelsang Th and Hofmann K R 1993 *Appl. Phys. Lett* **63** 186
[55] Basu P K and Paul S K 1992 *J. Appl. Phys.* **71** 3617
[56] Miyata H, Yamada T and Ferry D K 1993 *Appl. Phys. Lett.* **62** 2661
[57] Yamada T, Miyata H, Jhou J R and Ferry D K 1994 *Phys. Rev.* B **49** 1875
[58] Rashed M, Shih W K, Jallepalli S, Kwan T J T and Maziar C M 1995 *IEEE IEDM Tech. Dig.* 765
[59] Welser J, Hoyt J L, Takagi S and Gibbons J F 1994 *IEEE IEDM Tech. Dig.* 373
[60] Ismail K, Nelson S F, Chu J O and Meyerson B S 1993 *Appl. Phys. Lett.* **63** 660
[61] Gamiz F, Lopez-Villanueva J A, Roldan J B, Carceller J E and Cartujo P 1996 *ESSDERC 96 26th Eur. Solid State Development and Research Conf.* p 411
[62] Rim K, Welser J, Hoyt J L and Gibbons J F 1995 *IEEE IEDM Tech. Dig.* 517
[63] Nayak D K, Goto K, Yutani A, Murota J and Shiraki Y 1996 *IEEE Trans. Electron Devices* **43** 1709
[64] Nayak D K, Woo J C S, Park J S, Wang K L and MacWilliams K P 1993 *Appl. Phys. Lett.* **62** 2853
[65] Xie Y H, Fitzgerald E A, Monroe D, Silverman P J and Watson G P 1993 *J. Appl. Phys.* **73** 8364
[66] Mii Y J, Xie Y H, Fitzgerald E A, Monroe D, Thiel F A, Weir B and Feldman L C 1991 *Appl. Phys. Lett.* **59** 1611
[67] Schuberth G, Scaffler F, Besson M, Abstreiter G and Gornik E 1991 *Appl. Phys. Lett.* **59** 3318
[68] Ismail K, Meyerson B S and Wang P J 1991 *Appl. Phys. Lett.* **58** 2117
[69] Herzog H J, Jorke H and Schaffler F 1990 *Thin Solid Films* **184** 237
[70] Schaffler F 1993 *6th Int. Conf. on Modulated Semiconductor Structures* p 333
[71] Nayak D K and Shiraki Y 1995 *Properties of Strained and Relaxed Silicon Germanium* ed E Kasper (London: INSPEC) p 205
[72] Ismail K 1996 *J. Vac. Sci. Technol.* B **14** 2776
[73] Nelson S F, Ismail K, Chu J O and Meyerson B S 1993 *Appl. Phys. Lett.* **63** 367
[74] Ismail K, LeGoues F K, Saenger K L, Arafa M, Chu J O, Mooney P M and Meyerson B S 1994 *Phys. Rev. Lett.* **73** 3447
[75] Ismail K, Arafa M, Stern F, Chu J O and Meyerson B S 1995 *Appl. Phys. Lett.* **66** 842
[76] Ismail K, Arafa M, Saenger K L, Chu J O and Meyerson B S 1995 *Appl. Phys. Lett.* **66** 1077
[77] Garchery L, Warren P, Sagnes I and Badoz P A 1995 *Mater. Res. Soc. Symp. Proc.* **379** 321
[78] Whall T E, Smith D W, Plews A D, Kubiak R A, Phillips P J and Parker E H C 1993 *Semicond. Sci. Technol.* **8** 615

[79] Engelhardt C M, Tobben D, Aschauer M, Schaffler F, Abstreiter G and Gornik E 1993 *6th Int. Conf. on Modulated Semiconductor Structures* p 572
[80] van de Walle C G and Martin R M 1986 *Phys. Rev.* B **34** 5621
[81] Braunstein R, Moore A R and Herman F 1958 *Phys. Rev.* **109** 695
[82] Maiti C K, Bera L K, Dey S S, Nayak D K and Chakrabarti N B 1997 *Solid-State Electron.* **41** 1863
[83] Nelson S F, Ismail K, Jackson T N, Nocera J J and Chu J O 1993 *Appl. Phys. Lett.* **63** 794
[84] Ismail K, Meyerson B S, Rishton S, Chu J, Nelson S and Nocera J 1992 *IEEE Electron. Device Lett.* **13** 229
[85] Konig U, Boers A J, Schaffler F and Kasper E 1992 *Electron. Lett.* **28** 160
[86] Welser J, Hoyt J L and Gibbons J F 1993 *Proc. Int. Conf. on SSDM* p 377
[87] Bera L K, Ray S K, Nayak D K, Usami N, Shiraki Y and Maiti C K 1997 *Appl. Phys. Lett.* **70** 66
[88] Bera L K, Mukhopadhyay M, Ray S K, Nayak D K, Usami N, Shiraki Y and Maiti C K 1997 *Appl. Phys. Lett.* **70** 217
[89] Maiti B 1993 Novel thin dielectric devices and processing using low-pressure chemical vapor deposited films *PhD Thesis* The University of Texas at Austin
[90] Bera L K, Ray S K, Mukhopadhyay M, Nayak D K, Usami N, Shiraki Y and Maiti C K *IEEE Electron Device Lett.* submitted
[91] Maiti B, Hao M Y, Lee I and Lee J C 1992 *Appl. Phys. Lett.* **61** 1790
[92] Mukhopadhyay M, Ray S K and Maiti C K 1995 *Electron. Lett.* **22** 1953
[93] Hwang H, Ting W, Kong D L and Lee J 1990 *IEEE IEDM Tech. Dig.* 421
[94] Liu Z H, Wann H J, Ko P, Hu C and Cheng Y C 1992 *IEEE Electron Device Lett.* **13** 402
[95] Ray S K, Maiti C K, Lahiri S K and Chakrabarti N B 1992 *J. Vac. Sci. Technol.* B **10** 1139
[96] Bhat M, Yoon G W, Kim J and Kong D L 1994 *Appl. Phys. Lett.* **64** 2116
[97] Rao V R, Eisele I, Patrikar R M, Sharma D K, Vasi J and Grabolla T 1997 *IEEE Electron. Device Lett.* **18** 84
[98] Maiti B and Lee J C 1992 *Mater. Res. Soc. Symp. Proc.* **265** 255
[99] Arafa M, Fay P, Ismail K, Chu J O, Meyerson B S and Adesida I 1996 *IEEE Electron Device Lett.* **17** 124
[100] Chattopadhyay S, Bera L K, Ray S K and Maiti C K 1997 *Appl. Phys. Lett.* **71** 942
[101] Chattopadhyay S, Bera L K, Maharatna K, Chakrabarti S, Ray S K and Maiti C K 1997 *Solid-State Electron.* **41** 1891
[102] Chattopadhyay S, Bera L K, Ray S K, Bose P K and Maiti C K unpublished
[103] Daembkes H, Herzog H J, Jorke H, Kibbel H and Kasper E 1986 *IEEE Trans. Electron Devices* **33** 633
[104] Pearsall T P and Bean J C 1986 *IEEE Electron Device Lett.* 308
[105] Konig U and Schaffler F 1993 *Electron. Lett.* **29** 486
[106] Konig U and Schaffler F 1991 *Electron. Lett.* **27** 1405
[107] Konig U, Boers A J and Schaffler F 1993 *IEEE Electron Device Lett.* **14** 97
[108] Ismail K, Rishton S, Chu J O, Chan K and Meyerson B S 1993 *IEEE Electron Device Lett.* **14** 348
[109] Awano Y, Kosugi M, Mimura T and Abe M 1987 *IEEE Electron Device Lett.* **8** 451
[110] Arafa M, Fay P, Ismail K, Chu J O, Meyerson B S and Adesida I 1996 *IEEE Electron Device Lett.* **17** 449
[111] Ismail K 1995 *IEEE IEDM Tech. Dig.* 509
[112] Welser J, Hoyt J L and Gibbons J F 1994 *IEEE Electron Device Lett.* **15** 100
[113] Welser J, Hoyt J L and Gibbons J F 1992 *IEEE IEDM Tech. Dig.* 1000
[114] Chakrabarti N B, Mishra P P, Bera L K, Ghosh D and Maiti C K 1998 *Proc. Int. Conf. on Computers and Devices for Communication (Calcutta) (CODEC-98)* p 369
[115] Jones B K 1994 *IEEE Trans. Electron Devices* **41** 2188
[116] Armstrong G A and Maiti C K 1998 *Solid-State Electron.* **42** 487
[117] Abramo A, Bude J, Venturi F and Pinto M R 1996 *IEEE Electron Device Lett.* 59
[118] Armstrong G A, Uppal S and Maiti C K 1998 *Proc. Int. Conf. on Computers and Devices for Communication (Calcutta) (CODEC-98)* p 385
[119] Fischetti M V and Laux S 1993 *Phys. Rev.* B **48** 2244
[120] Vogelsang T, Hofmann F, Schafer H, Risch L and Hofmann K 1994 *Ext. Abstr. Conf. on Solid State Devices and Materials* p 877
[121] Arora N D, Hauser J R and Roulston D J 1982 *IEEE Trans. Electron Devices* **29** 292
[122] Clifton P A, Routley P R, Gurry P K, O'Neill A G, Carter J A and Kemhadjian H A 1996 *ESSDERC 96 26th Eur. Solid State Dev. Res. Conf.* p 519
[123] Sadek A, Ismail K, Armstrong M A, Antoniadis D A and Stern F 1996 *IEEE Trans. Electron Devices* **43** 1224
[124] O'Neill A G and Antoniadis D A 1996 *IEEE Trans. Electron Devices* **43** 911
[125] O'Neill A G and Antoniadis D A 1997 *IEEE Trans. Electron Devices* **44** 80
[126] Armstrong M A, Antoniadis D A, Sadek A, Ismail K and Stern F 1995 *IEEE IEDM Tech. Dig.* 761
[127] Ismail K, Chu J O and Meyerson B S 1994 *Appl. Phys. Lett.* **64** 3124
[128] Lee K F, Yan R H, Jeon D Y, Chin G M, Kim Y O, Tennant D M, Razavi B, Lin H D, Wey Y G, Westerwick E H, Morris M D, Johnson R W, Liu T M, Tarsia M, Cerullo M, Swartz R G and Ourmazd A 1993 *IEEE IEDM Tech. Dig.* 131
[129] Taur Y, Wind S, Mii Y, Lii Y, Moy D, Jenkins K A, Chen C L, Coane P J, Klaus D, Bucchignano J, Rosenfield M, Thomson M G R and Polcari M 1993 *IEEE IEDM Tech. Dig.* 127
[130] Gluck M, Hackbart T, Konig U, Hass A, Hock G and Kohn E 1997 *Electron. Lett.* **33** 335
[131] Konig U and Schaffler F 1993 *IEEE Electron Device Lett.* **14** 205